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Transistors based on two-dimensional materials for future integrated circuits

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Field-effect transistors based on two-dimensional (2D) materials have the potential to be used in very large-scale integration (VLSI) technology, but whether they can be used at the front end of line or at the back end of line through monolithic or heterogeneous integration remains to be determined. To achieve this, multiple challenges must be overcome, including reducing the contact resistance, developing stable and controllable doping schemes, advancing mobility engineering and improving high-κ dielectric integration. The large-area growth of uniform 2D layers is also required to ensure low defect density, low device-to-device variation and clean interfaces. Here we review the development of 2D field-effect transistors for use in future VLSI technologies. We consider the key performance indicators for aggressively scaled 2D transistors and discuss how these should be extracted and reported. We also highlight potential applications of 2D transistors in conventional micro/nanoelectronics, neuromorphic computing, advanced sensing, data storage and future interconnect technologies.

The scaling of silicon complementary metal–oxide–semiconductor (CMOS) technology has reached sub-10-nm technology nodes, but further scaling is increasingly challenging because the gate electrostatics of the devices demand an aggressive reduction in channel thickness to preserve the desired performance[1]. The ultimate channel thickness for a field-effect transistor (FET) is potentially in the sub-1-nm range. However, this is not readily accessible for any three-dimensional (3D) semiconducting crystal because of increased scattering of charge carriers at the channel-to-dielectric interfaces, which leads to severe mobility degradation[2].

Two-dimensional (2D) semiconducting materials, which in monolayer form have a thickness of ~0.6 nm, could provide a solution. Such materials include transition metal dichalcogenides (TMDs) with the general formula MX_2, where M is a transition metal (for example, Mo or W) and X is a chalcogen (for example, S, Se or Te)[3–8]. The absence of dangling bonds in the materials also offers the potential to achieve better channel-to-dielectric interfaces. Early studies based on mechanically exfoliated single-crystalline 2D flakes, and more recent developments based on large-area grown synthetic 2D monolayers, have illustrated the promising characteristics of 2D transistors. However, the multitude of challenges that remain to be solved makes the potential incorporation of 2D FETs in future very large-scale integration (VLSI) technologies far from clear.

In this Review, we explore the development of 2D FETs for future integrated circuits. We first consider the large-area growth of 2D channel materials and the fabrication of a 2D FET, as well as the extraction of key parameters for a comprehensive assessment of device performance. We emphasize the importance of studying the device-to-device variation, stability and reliability of the 2D FETs. We then assess the key challenges that must be addressed to achieve VLSI applications based on 2D FETs. These include reducing the contact resistance R_C, achieving stable doping, advancing mobility engineering and improving the integration of high-κ dielectrics (where κ is the dielectric constant). Finally, we highlight potential applications of 2D FETs in digital and analogue electronics, memory, neuromorphic computing, sensing devices and interconnect technology.

Fundamentals of 2D material processing

Early demonstrations of 2D FETs were based on micromechanically exfoliated flakes[9]. Although the exfoliation technique lacks scalability and manufacturability, it enables rapid experimental screening of different 2D materials and serves as a testbed for device optimization and applications. It also helps to check the compatibility of 2D materials with standard processing techniques. However, for VLSI integration of 2D FETs, wafer-scale synthesis is unavoidable and chemical vapour deposition (CVD) and metal–organic CVD (MOCVD) techniques are the forerunners in this context[10]. Figure 1a shows MOCVD-grown MoS_2, $MoSe_2$, WS_2 and WSe_2 on two-inch sapphire wafers[11]. Although the most important growth parameter is the process temperature, which is typically >500 °C,

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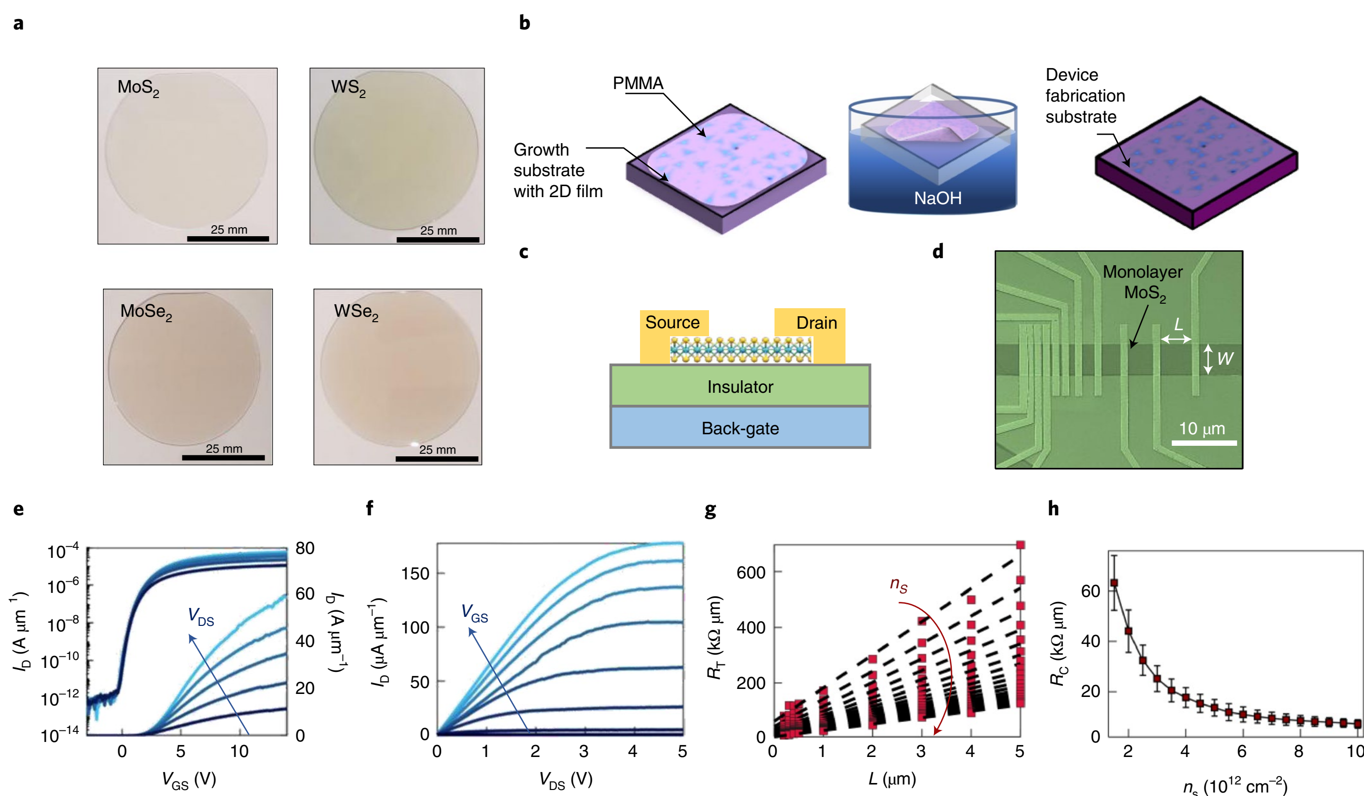


Fig. 1 | Two-dimensional FET fabrication and characterization. **a**, Epitaxial large-area growth of highly crystalline 2D monolayers on a sapphire substrate using a MOCVD technique by the Two-Dimensional Crystal Consortium (2DCC), an initiative of the National Science Foundation (NSF) through the Materials Innovation Platform (MIP)[11]. **b**, The poly(methyl methacrylate) (PMMA)-based wet-transfer technique developed by Zhang and others[18]. **c**, Schematic of a 2D FET with global back-gate. **d**, SEM image of a TLM structure fabricated on monolayer MoS_2. The channel is etched in a rectangular geometry to ensure constant channel width W. **e**,**f**, Transfer characteristics (that is, source-to-drain current, I_D) measured by sweeping the gate voltage (V_{GS}) at constant drain voltage (V_{DS}), plotted in linear and logarithmic scale (**e**) and output characteristics obtained by measuring I_D by sweeping V_{DS} at constant V_{GS} (**f**) of a 2D FET based on MOCVD-grown monolayer MoS_2. I_D is reported in units of $\mu A\,\mu m^{-1}$ by normalizing to W. **g**, Total channel resistance (R_T) as a function of channel length (L) for different carrier concentrations (n_S) obtained from a TLM geometry for monolayer MoS_2 with a 30 nm Ni/40 nm Au contact. Contact resistance (R_C) can be extracted from the x intercept of the linear fit of R_T versus L following Supplementary equation (5). **h**, R_C versus n_S obtained from 23 TLM structures. The error bars show the median and the interval between 25th percentile and 75th percentile. Panel **a** reproduced with permission from ref. [11], Pennsylvania State University. Panels **d**–**h** adapted with permission from ref. [125] under a Creative Commons licence CC BY 4.0.

the choice of precursors and substrate can also influence the growth. For example, crystalline substrates such as sapphire can facilitate the epitaxial growth of TMDs, which greatly reduces the number of grain boundaries and improves the performance of the 2D FETs[12]. Note that 2D FETs must meet the performance criterion set forth by the International Roadmap for Devices and Systems (IRDS) for consideration as front end-of-line (FEOL) devices in advanced nodes, as discussed later. The performance criterion is less stringent for back end-of-line (BEOL) devices[13], but CMOS process compatibility necessitates low-temperature growth (<450 °C) of TMDs, which is non-trivial[14] and requires further investigation beyond some initial demonstrations[15,16]. Alternatively, temperature- and substrate-related constraints of monolithic integration can be avoided by growing TMDs on desired substrates with higher thermal budgets, followed by clean and damage-free large-area transfers[17]. Figure 1b shows a commonly used wet-transfer technique developed by Zhang and others[18].

Fabrication of 2D FETs. Fabrication of all layers required for 2D FETs must be clean and free from mechanical damage during the various lithography, etching and deposition processes. Photoresist residues can be removed by thermal/current annealing post device fabrication and by plasma treatment before depositing the contacts[19,20]. However, plasma treatment can damage the underlying 2D materials. Easily removable sacrificial metal/polymer layers can also be used with standard lithography techniques to reduce photoresist residue[21]. Note that, for 300 mm integration, it is likely that a different integration scheme will be adopted that no longer relies on liftoff techniques[22]. Figure 1c presents a schematic of a 2D FET with the most commonly used global back-gate geometry and Fig. 1d shows a scanning electron microscopy (SEM) image of a transmission line measurement (TLM) structure. Note that the monolayer MoS_2 film is etched into a rectangular shape to ensure constant channel width W, which is recommended practice. However, as the channel width becomes narrower at advanced VLSI nodes, dangling bonds at the edges must be passivated accordingly. Finally, for VLSI integration, individually controllable dual-gated 2D FETs are required. Such structures have been investigated in the form of standard top-gated[23,24], split-gated[25] and gate-all-around[26] geometries.

Electrical characterization of 2D FETs. Good practice for 2D FET characterization should take into account the following protocols. It has been shown that the electrical characteristics of as-fabricated 2D FETs drift and change under repeated testing. Therefore, it is recommended that the measurement conditions are stabilized by controlled biasing schemes before key device parameters are extracted and the procedure is reported accordingly. Standard measurements of 2D FETs include the transfer characteristics (that is,

measuring the drain current (I_D) while sweeping the source-to-gate voltage (V_{GS}) at constant source-to-drain voltage (V_{DS}) plotted in linear and logarithmic scale, Fig. 1e) and output characteristics obtained by measuring I_D while sweeping V_{DS} at constant V_{GS} (Fig. 1f). I_D should be reported in units of $\mu A\,\mu m^{-1}$ by normalizing to the width of the 2D channel (W). The gate leakage current (I_G) should also be reported to ensure that I_D is free from any artefacts. It is also recommended that the voltage sweeps are performed in both directions, for different sweep rates and sweep ranges, to reveal the hysteresis in the device characteristics[27]. As detailed in the following, a comprehensive report on device performance indicators must include the off current (I_{OFF}), on current (I_{ON}), current on/off ratio, threshold voltage (V_{TH}), carrier mobility (μ), inverse subthreshold slope (SS), contact resistance (R_C) and saturation velocity (v_{SAT}).

I_{OFF} is often determined by the noise floor of the measurement instrument if not stated otherwise. For I_{ON}, it is important to specify V_{DS} and the gate overdrive voltage ($V_{GS} - V_{TH}$) or the carrier concentration n_S (Supplementary Section 1 provides a discussion of the extraction of n_S). The current on/off ratio must be stated for a given gate voltage range ($V_{GS,max} - V_{GS,min}$). V_{TH} can be extracted using linear extrapolation ($V_{TH_{lin}}$) of the transfer characteristics[28], the Y-function method (V_{TH_Y})[29] or the constant-current method ($V_{TH_{cc}}$)[28] (Supplementary Section 2 provides an illustration of the extraction of V_{TH} by different methods). Note that V_{TH} will differ depending on the extraction method, so the method should be reported accordingly. Carrier mobility (μ) can be extracted from the peak transconductance (μ_{g_m}), Y-function (μ_Y) or TLM (μ_{TLM}) (Supplementary Section 2 presents further discussion on mobility extraction)[30]. SS should be reported as an average over several orders of magnitude change in I_D. Although the expected SS for any ultrathin-body (UTB) FET is $60\,mV\,dec^{-1}$, this value is rarely achieved in 2D FETs due to the finite interface trap capacitance (C_{IT}) given by the interface trap density, D_{IT} (Supplementary Section 2)[31]. R_C is extracted using the TLM geometry for different n_S using Fig. 1g and Supplementary equation (5) as shown in Fig. 1h. Note that, unlike silicon FETs, where metal–silicon interfaces are mostly ohmic in nature owing to the formation of metal silicide, metal–2D interfaces are mostly Schottky in nature, with the Schottky barrier (SB) width being a function of V_{GS} (refs. [29,32]). Furthermore, for silicon FETs, the channel underneath the metal contacts is degenerately doped and hence cannot be gated, whereas the 2D channels are mostly intrinsic and are under gate control in a back-gated geometry[29,32]. As a result, the value of R_C in 2D FETs depends on ($V_{GS} - V_{TH}$) or n_S and must be reported accordingly (Fig. 1h). For a more comprehensive understanding of metal–2D contacts, temperature-dependent measurements must be performed to extract the SB height[32–34].

Saturation velocity (v_{SAT}) is another important parameter for FETs. Although, at low lateral electric field E, the average electron or hole drift velocity (v_d) increases linearly with mobility following $v_d = \mu E$, at large electric field the carrier velocity saturates. In silicon, $v_{sat} \approx 10^7\,cm\,s^{-1}$ occurs at $E > 1\,V\,\mu m^{-1}$ (ref. [35]), a value that is readily achievable in submicrometre FETs. Thus, I_{ON} becomes less dependent on μ and is instead proportional to v_{sat}, following $I_{ON} = qn_S v_{sat}$ (ref. [36]). Recently, Nathawat et al.[37] reported $v_{sat} \approx 6\times10^6\,cm\,s^{-1}$ for MoS_2 on SiO_2 using a pulsed measurement technique. If this average velocity were maintained along the channel of a MoS_2 transistor, $I_{ON} \geq 1\,mA\,\mu m^{-1}$ could be achieved in this monolayer semiconductor at a carrier density of $n_S \geq 10^{13}\,cm^{-2}$ (Supplementary Section 3 provides more discussion about v_{sat}). Figure 2a summarizes the experimental results for v_{sat} in various 2D and 3D materials[38].

Note that, during the measurement of a 2D FET, particularly with thicker back-gate oxides, current saturation can occur through either pinch-off or velocity saturation and self-heating (SH), as illustrated in Fig. 2b. In the former case, the saturation current has a classical[35] quadratic dependence, $(V_{GS} - V_{TH})^2$, whereas in the latter case the current scales linearly[36] or even sublinearly (when SH becomes non-negligible[38]) with ($V_{GS} - V_{TH}$). SH is a challenge because it degrades transistor performance and reliability, and because it introduces complications for interpretation of the high-field device parameters, such as v_{sat}. SH plays an important role in 2D FETs, which are an extreme case of semiconductor-on-insulator (SOI) technology[38], because the 2D channel is often on a thermally resistive film of SiO_2. In addition, the weak van der Waals interface with SiO_2 has a relatively large thermal boundary resistance (TBR $\approx 60\,m^2\,K\,GW^{-1}$), equivalent to the thermal resistance of ~80 nm SiO_2 at room temperature[39,40]. Direct thermal measurements of MoS_2 FETs have found that their temperature rise can exceed ~200 °C during operation[40].

SH in 2D FETs can be identified from the output characteristics (Fig. 2c). First, we note a sublinear dependence of the saturation current on ($V_{GS} - V_{TH}$) is distinct from the linear relationship due to velocity saturation or the quadratic dependence due to classical pinch-off. Second, extreme SH can lead to negative differential conductance (NDC) at high current levels, which has also been observed in measurements taken at sufficiently high V_{DS} (and I_D)[41]. Both effects are caused by increased scattering as the temperature increases during high-current operation. Several measures can be taken to limit SH effects in 2D transistors. First, a reduction of the channel length increases thermal dissipation into the metal contacts[39,42]. Second, switching transistors with nanosecond (or faster) pulses[37] reduces SH by operating them below the thermal time constant[43], which can be on the order of ~100 ns. Third, the thermal resistance could be reduced by decreasing the insulator thickness (or using hexagonal boron nitride (hBN) as a lateral heat spreader[44]) and improving the TBR of the interfaces surrounding the 2D material. Supplementary Section 4 provides more discussion of SH.

The importance of mobility. Note that carrier mobility is less important for ultra-scaled devices than is often assumed because the terminal currents in nanoscale transistors are limited by R_C (refs. [30,38,45,46]), v_{sat} (when optical phonon scattering dominates[36]) or injection velocity (in ultrashort channels comparable to the scattering mean free path[47]). Still, mobility is a useful quantity to estimate electron or hole scattering rates and effective masses at a given temperature (for scattering with phonons), carrier density (Coulomb screening effects), channel thickness (surface roughness) and gate insulator properties (remote phonon and impurity scattering). However, because mobility, unlike current, is never measured directly, its extraction can be prone to substantial errors.

So, what is more important for transistor performance—current (high I_{ON} and low I_{OFF}), high transconductance (g_m), low output conductance (g_o) or low parasitic capacitance? As an example, Fig. 2d displays I_{ON} from measurements of monolayer MoS_2 transistors[38,46,48–55] as a function of L, at the same $V_{DS} = 1\,V$ and maximum V_{GS} reported. The solid curves represent a simple model with $I_{ON} = V_{DS}/(LR_{sh} + 2R_C)$, where $R_{sh} = (qn_S\mu)^{-1} \approx 8\,k\Omega\,sq^{-1}$ is the average channel sheet resistance with $n_S = 2\times10^{13}\,cm^{-2}$, $\mu = 40\,cm^2\,V^{-1}\,s^{-1}$ and $R_C = 1\,k\Omega\,\mu m$ or $500\,\Omega\,\mu m$, in the range of the best contacts reported so far[30,38,45,46]. Micrometre-scale transistors are limited by their mobility or saturation velocity[38], but short channels ($L < 2R_C/R_{sh}$, especially <100 nm) are strongly limited by their contacts. Thus, the largest improvements of short-channel MoS_2 transistors will be achieved by further reducing the contact resistance, together with reduction of the effective oxide thickness (EOT). Other benchmarking data for multilayer and other 2D material transistors are available on a recently launched website[52].

Insulators and reliability. A prerequisite for 2D FETs to be considered mature enough for VLSI applications is that they operate reliably over their entire lifetime of typically 10 years. Different methodologies provide different perspectives on how the reliability of 2D

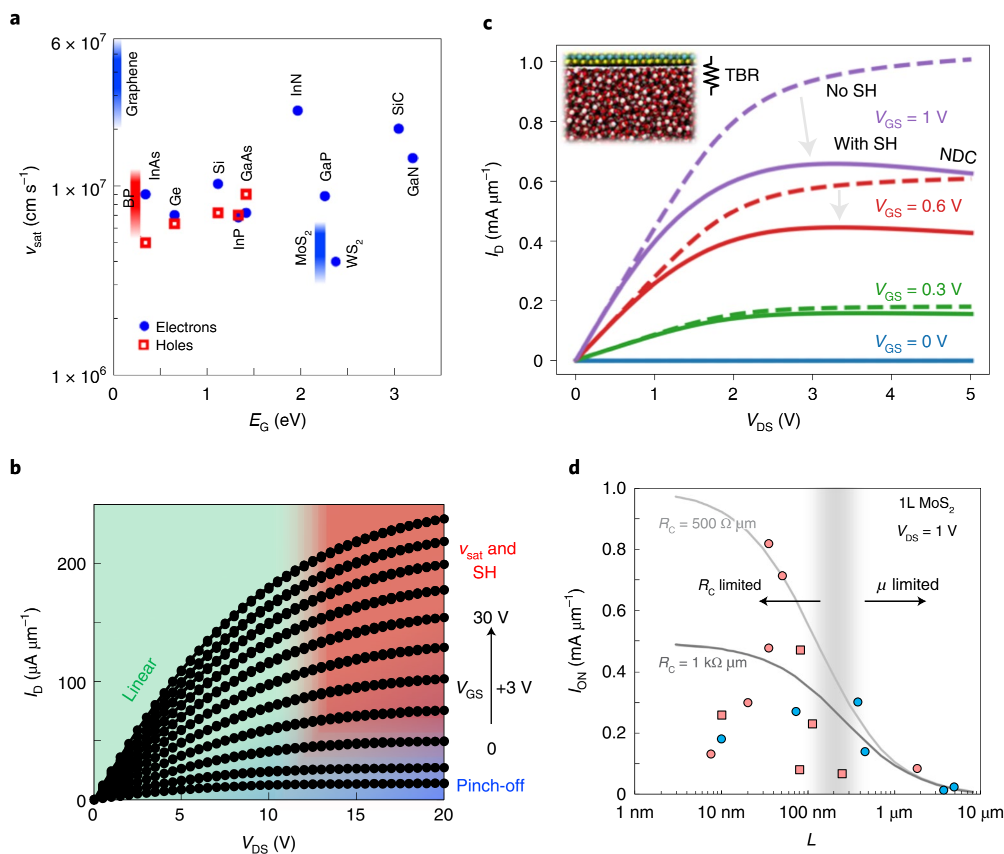


Fig. 2 | Saturation current and saturation velocity in 2D FETs. a, Summary of measured saturation velocity (v_{sat}) versus bandgap (E_G) in various 2D and 3D materials[38]. Some values are shown as ranges, with the lower end representing values that are limited by SH and remote phonon scattering, and the top end corresponding to values obtained from pulsed measurements[37] or samples with better heat sinking (for example, on hBN[44]). BP, black phosphorus. **b**, Measurements of a back-gated monolayer MoS_2 transistor ($L = 4.9$ µm on $t_{OX} = 30$ nm SiO_2, where t_{OX} is the gate insulator thickness) illustrating three regimes of operation[38]. **c**, Simulated monolayer MoS_2 transistor output curves including (solid lines) and excluding SH (dashed). Channel length $L = 200$ nm and EOT = 1 nm. For simplicity, the thermal resistance is assumed to be entirely limited by the TBR of the MoS_2/SiO_2 interface (inset)[184]. SH can cause ~40% current reduction and NDC (also seen experimentally[38]) at the highest power densities simulated here. **d**, Measured current of monolayer MoS_2 transistors (symbols) versus channel length[52], compared with a simple model (lines) at $V_{DS} = 1$ V. The gate voltage V_{GS} is at the maximum reported in the respective experimental study. The measurements were conducted in a room-temperature environment, but the temperature at the point of maximum current (shown here) could be a few hundred degrees higher, due to SH[39,40]. Circles show measurements for back-gated devices and squares the measurements for top- or dual-gated devices. Blue filled symbols indicate a SiO_2 gate insulator and rose filled symbols higher-κ insulators. Panels **a** and **b** adapted with permission from ref. [38], American Chemical Society.

devices is adversely affected by inferior semiconductor-to-insulator interfaces as well as insulator defects. Valuable insights can be gained about the semiconductor-to-insulator interface from studying low-frequency variations (millihertz to megahertz) in I_D—commonly called flicker or $1/f$ noise[56,57]. The magnitude of the noise spectral density determines the precision limit of FET operation, which can be increased by eliminating charge traps in the vicinity of the channel, either via encapsulation[57] or by including hBN between the substrate and the 2D channel[56]. The same charge traps can be studied on an atomic level in nanoscale FETs, where the number of traps per device can be reduced from several thousand down to a countable number of less than 100. In this case, the current fluctuations take the form of discrete steps, as every single trapping event triggers a discrete step in I_D, which is called random telegraph noise (RTN). So far, the technological difficulty of fabricating high-quality 2D FETs with a sufficiently small charge trap or defect density ($N_T < 10^{12}$ cm^{-2}) and active area ($A < 100$ nm × 100 nm), which together determine the total number of defects ($N = N_T \times A$), has limited the number of studies on RTN in 2D FETs[58,59]. The location of the defects has been analysed, confirming that the most detrimental charge traps are located at adsorbates and in the gate insulator[59]. Figure 3a shows the atomic structure of the MoS_2/SiO_2 interface (left), which is more defective than the Si/SiO_2 interface (right). Most importantly, the average time constants of the traps cover an extremely wide range, from nanoseconds (and probably faster) to years (Fig. 3b).

In addition to noise, the charge-trapping events at insulator defects in the vicinity of the channel cause a hysteresis in the transfer characteristics of 2D FETs[27,60,61] that can be orders of magnitude larger than what is observed in commercial silicon technologies[62]. Charge trapping can also cause an apparent SS of <60 mV dec^{-1} during the 2D FET transfer characteristics measurements, as shown for oxide-based FETs[63]. Detailed studies have revealed that the critical defects are located in the insulator ~1–5 nm (ref. [64]) away from the channel, which classifies them as border traps. In addition to border traps, water and other gaseous adsorbates from an ambient environment[60] or residue from immature processing at the critical semiconductor-to-insulator interface will substantially increase the observed hysteresis. Typically, the hysteresis increases with increasing voltage ranges[27] and sweep times[61].

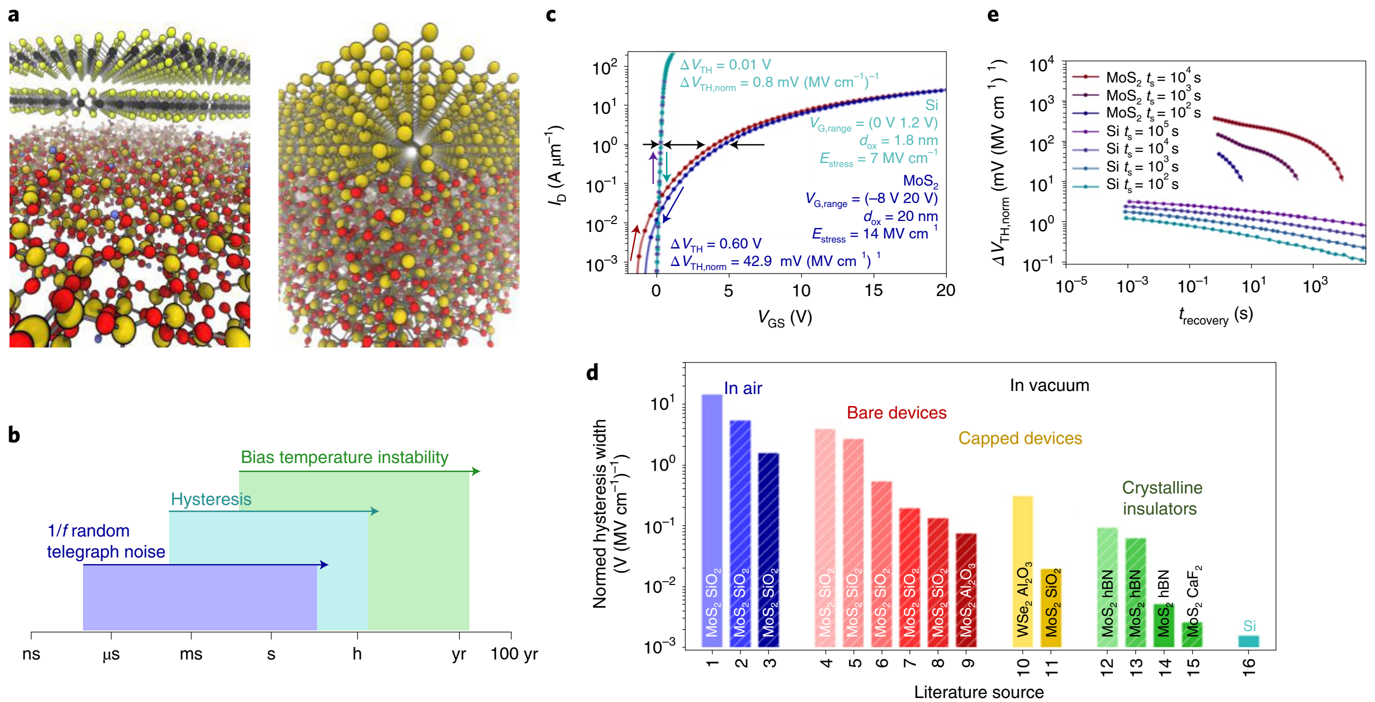


Fig. 3 | Reliability of 2D FETs. a, The atomic structure of the MoS_2/SiO_2 interface (left) contains many hydrogen atoms (shown in blue) and dangling bonds, resulting in a defective interface. By comparison, the Si/SiO_2 interface (right) is notably less defective. **b**, Charge-trapping time constants associated with RTN, hysteresis and BTI cover an extremely wide range and are only accessible by measurements that combine different methods. **c**, Comparison of the hysteresis width for Si/SiO_2 (ref. [62]) and MoS_2/SiO_2 (ref. [185]). **d**, Hysteresis widths measured on 16 different 2D FETs: 1, ref. [186]; 2, ref. [60] (in air); 3, ref. [187]; 4, ref. [188] (SiO_2); 5, ref. [60] (in vacuum); 6, ref. [27] (SiO_2); 7, ref. [185] (bare); 8, ref. [64]; 9, ref. [188] (Al_2O_3); 10, ref. [189]; 11, ref. [185] (capped); 12, ref. [27] (hBN); 13, ref. [61] (bare); 14, ref. [61] (capped); 15, ref. [65]; 16, ref. [62]. Bars with white stripes indicate that the respective devices were back-gated with a bare channel. **e**, Negative BTI measured in Si/SiO_2 (ref. [190]) and MoS_2/SiO_2 (ref. [185]) FETs. Here, t_s is the stress time.

This knowledge can be exploited with a pulsed measurement scheme, where the hysteresis is considerably decreased for pulses in the millisecond range[64]. To reduce the density of border traps, a less defective gate insulator, for example, a multilayer hBN crystal[27,61] or ionic CaF_2 (ref. [65]), can be used. The hysteresis in two example devices is shown in Fig. 3c and the hysteresis width is compared for many different devices in Fig. 3d. Although the hysteresis has to be avoided for stable FET operation, it is useful for neuromorphic circuits[66], and the sensitivity of the hysteresis on the gas concentration can be exploited in gas sensors[67].

In addition to hysteresis, slower border traps can charge during device operation, thereby causing a shift of the threshold voltage, which, over time, accumulates until the operating point changes too much and the device fails[68,69]. This phenomenon is typically referred to as bias temperature instability (BTI). For BTI characterization, a gate bias is applied for a certain time and the shift of the threshold voltage (ΔV_{TH}) is recorded during the stress and recovery phases. Several studies have evaluated the BTI characteristics of 2D FETs[27,68,69] (Fig. 3e), where accelerated degradation was observed for stress-recovery measurements at elevated temperatures, typically between 40 °C and 200 °C (refs. [27,68,69]). Recovery traces contain valuable information on the permanence of the device degradation inflicted by gate bias stress[69].

Another reliability issue that is related to device failure towards the end of the lifetime is time-dependent dielectric breakdown (TDDB)[70]. TDDB depends primarily on the gate insulator as its physical mechanism is governed by the formation of defects in the insulator. Once the defect density crosses a critical threshold, a conductive filament is formed, which leads to a strong increase in the gate leakage current[70]. Contrary to the well-studied breakdown of SiO_2, 2D insulators have been shown to break down in a layer-by-layer fashion[71]. Even though TDDB needs to be avoided to provide stable FET operation, the physical mechanisms eventually leading to breakdown can be used to build resistive random-access memories[72].

An additional reliability concern is degradation caused by applying a high voltage at the drain side of the device—the so-called hot carrier degradation (HCD). Although HCD in silicon FETs is among the central reliability concerns in scaled devices[73], only very little is known about HCD in 2D material-based devices[74]; HCD may be fundamental for functionalized 2D materials or hydrogen-passivated edges, as these bonds could be susceptible to hot carrier-triggered dissociation.

The aforementioned reliability issues—1/*f* noise, RTN, hysteresis, BTI, TDDB and HCD—have a common root cause, namely charge-trapping events at defects and the formation of new defects at suitable defect precursor sites such as strained or dangling bonds in the vicinity of the 2D channel material. As a consequence, the typically highly defective interface between the 2D semiconductor and conventional 3D oxides, such as SiO_2 or HfO_2, which additionally contain high numbers of intrinsic defects, will result in poor reliability. The border traps in the insulator are energetically aligned within distinct defect bands that are broader in amorphous oxides and tend to degenerate to discrete levels in crystalline insulators[31]. This could help in solving the reliability challenges of 2D FETs by using less defective, crystalline insulators, which offer the possibility of forming a (quasi) van der Waals interface with the 2D semiconductor in the channel[31]. From our current perspective, the most promising candidates for this purpose are layered 2D insulators such as hBN[61], mica[75], native layered oxides like Bi_2SeO_5 (ref. [76]) or

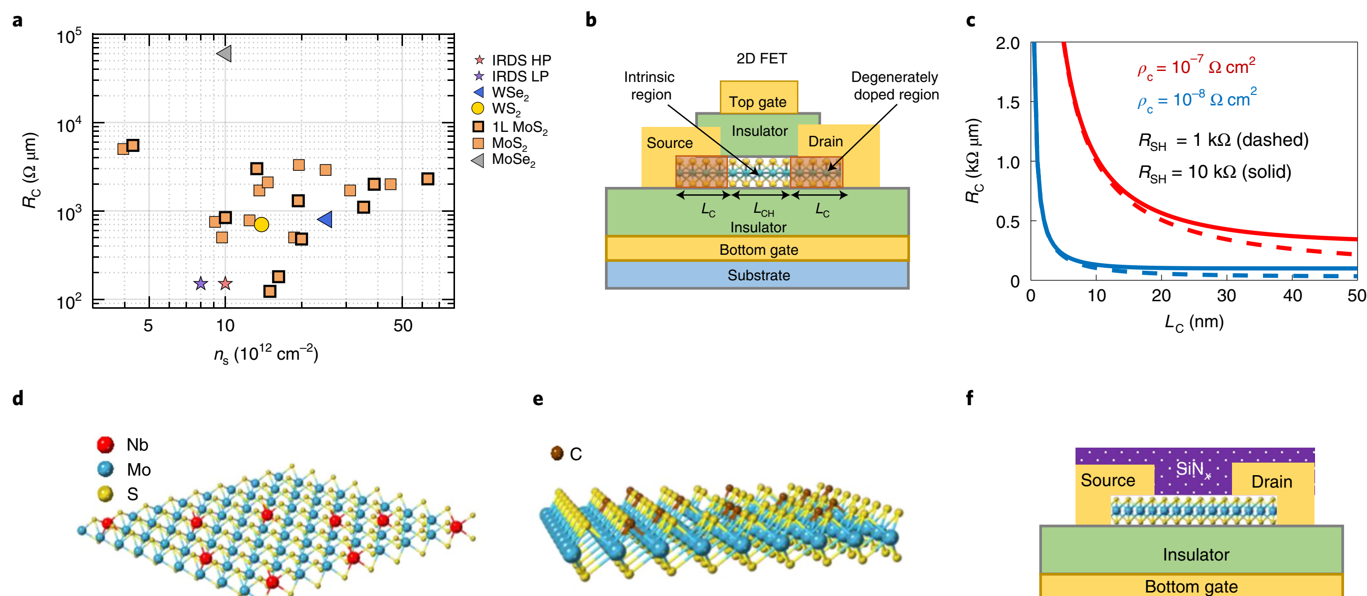


Fig. 4 | Contact resistance and doping of 2D FETs. a, Some of the best reports for R_C for different TMDs, along with the IRDS requirements for HP and LP FETs in future VLSI technology nodes[52]. **b**, Device layout for dual-gated 2D FETs to avoid, in particular, overlap capacitances between the source–drain metal contacts and the gate that are currently present in almost all prototype 2D FETs. Both n-type and p-type 2D FETs need to be developed with degenerate doping underneath the source–drain contacts, with the gate operating on the intrinsic region. Doped regions can also be replaced with metallic 2D materials. **c**, Calculated R_C versus L_C for different combinations of ρ_C and R_{SH} (ref. [81]). R_C increases monotonically as L_C is scaled down. **d**, Substitutional Nb-doping of MoS_2 during growth. **e**, C-doping, post growth, of monolayer MoS_2 using plasma. **f**, Schematic of a back-gated 2D FET with silicon nitride (SiN_x) as the SCTD layer. Panel **a** adapted with permission from ref. [52], Stanford University.

fluorides such as CaF_2 (ref. [65]). Even so, the introduction of such new insulators poses its own challenges related to the growth of crystalline insulators at a moderate thermal budget or other important insulator requirements such as a high dielectric constant (see the section 'Dielectric integration'). Nevertheless, many of the reliability problems that might inhibit the use of 2D FETs in VLSI chips can at the same time be used to build 2D material-based devices, such as non-volatile memory elements[72], synaptic devices for neuromorphic computing[66] or highly sensitive sensors[77], as outlined in more detail in the section 'Potential applications for 2D FETs in future VLSI'.

Key technological challenges for 2D transistors

According to the IRDS for scaled FETs, 2D materials are a possible solution for the challenges faced in the technology nodes beyond 2028, that is, at the ultimate scaling limit[78]. The IRDS roadmap places stringent requirements on every technology that aims for these ultra-scaled dimensions, the most critical among them being low contact resistances, gate lengths on the order of 10 nm (ref. [55]), on currents in the range of 100 μA μm^{-1}–1 mA μm^{-1}, an inversion layer thickness of only 0.9 nm, off-state currents of 10 nA μm^{-1} for high-performance (HP) and 100 pA μm^{-1} for low-power (LP) requirements and competitive device reliability[78]. Here, we discuss the state of the art in 2D material-based nanoelectronics focusing on these aspects.

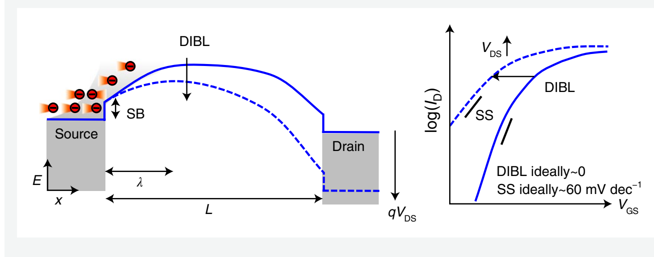
Contact resistance. Contact resistance holds the key to achieving high-performance 2D FETs. According to the IRDS 2020 Update[78], the total parasitic series resistance (R_{SD}) must be reduced to 221 Ω μm over the course of the next 15 years. Note that, for silicon transistors, $R_{SD} = 2R_C + 2R_A$, where R_C is the contact resistance and R_A is the access resistance, which includes contributions from the accumulation layer, spreading resistance and sheet resistance of the source–drain. The best R_C values for 2D FETs reported so far are ~123 Ω μm for a bismuth-contacted n-MoS_2 monolayer[53], ~180 Ω μm for n-channel monolayer MoS_2 (Ag/Au contact) after amorphous titanium suboxide (ATO) doping[54], and ~100 Ω μm for p-channel multilayer WSe_2 after nitric oxide (NO) doping (unpublished). Figure 4a summarizes some of the best reports of contact resistance for different TMDs[52]. Fundamental challenges in achieving low contact resistance in 2D FETs stem from the existence of a SB at the metal–2D interface, metal oxidation, metal reaction and damage to the 2D material, incomplete coverage due to metal grains and so on[32]. Attempts have been made to lower the SB height through metal work-function engineering, 2D/2D contacting and depinning of the Fermi level using interlayer insertion, as well as narrowing the SB width through surface charge transfer doping (SCTD)[32]. Although impressive, most approaches lack scalability for VLSI. In fact, high-performance n- or p-type 2D FETs with on currents approaching the mA μm^{-1} regime (to rival current silicon technology) with an inverse SS in the 60 mV dec^{-1} regime and a sufficiently low off current at supply voltages V_{DD} of ~1 V have not yet been achieved.

Future generations of 2D FETs will require a device layout as shown in Fig. 4b to avoid the overlap capacitances between electrodes that are currently present in almost all prototype 2D devices. In other words, both n- and p-type 2D FETs need to be developed with degenerate doping underneath the contacts and the gate operating on the intrinsic region. Some attempts at designing such a doping profile have been made[79], but the device performance remains inadequate. Conventional substitutional doping by means of ion implantation is undesirable because of probable damage to the ultrathin 2D channel, so SCTD or in situ growth approaches need to be employed. Another alternative could be making contact to phase-engineered metallic 2D materials[80].

Contact scaling is another important consideration for 2D FETs because nanoscale devices also require nanoscale contacts. As shown in Fig. 4c, R_C increases as the contact length (L_C) is reduced following

Box 1 | Drain-induced barrier lowering and scale length and short-channel effects

The left panel shows the conduction band edge versus position along the channel of an n-type 2D transistor below threshold, illustrating the electrostatic scale length λ and the DIBL phenomenon. Most 2D FETs have non-zero contact SB, as shown. Electrons are shown as small red particles in the source, entering the channel as the channel barrier is lowered. The right panel shows I_D versus V_{GS}, illustrating lower V_{TH} and worse SS due to DIBL at higher V_{DS}. The solid lines are at low V_{DS} and the dashed lines are with high V_{DS} in both panels. DIBL is minimized when $L > 3$ to 4λ. A common approximation of this scale length in SOI transistors[191] is $\lambda \approx \sqrt{\varepsilon_S t_S t_{OX}/\varepsilon_{OX}}$; however, this expression must be revisited when one of the thicknesses is much larger than the other. For example, in 2D FETs with $t_S \ll t_{OX}$, most electric fields from the drain traverse the insulator instead of the semiconductor body. The scale length also depends on FET geometry, for example, single- versus double-gate, gated versus doped contacts, isotropic versus anisotropic material permittivity. For a symmetric double-gate FET[192,193], the scale length is a solution of $\tan(t_S/2\lambda)\tan(t_{OX}/\lambda) = \varepsilon_{OX}/\varepsilon_S$, where the first term becomes linear in t_S for $t_S \ll \lambda$, as in monolayer 2D FETs. In this case, t_S is at the atomic limit and can no longer be scaled down, so t_{OX} remains the main parameter that must be reduced to prevent short-channel effects.



the expression $R_C = \sqrt{\rho_C R_{SH}}\coth(L_C/L_T)$, where, ρ_C is the specific contact resistivity, R_{SH} is the channel sheet resistance under the contact and $L_T = \sqrt{\rho_C/R_{SH}}$ is the transfer length, which determines the extent of current crowding[32,81]. For $L_C \gg L_T$, $R_C = \sqrt{\rho_C R_{SH}}$, independent of L_C, whereas, for $L_C \ll L_T$, $R_C = \rho_C/L_C$. Therefore, true reduction in R_C for aggressively scaled devices necessitates L_T scaling and/or reduction in ρ_C. To achieve $L_T < 10$ nm, $\rho_C \approx 10^{-8}\,\Omega\,cm^2$ must be achieved when $R_{SH} \approx 10\,k\Omega\,sq^{-1}$. Even for the best reported R_C for the TMDs, ρ_C is still about an order of magnitude higher than for heavily doped silicon contacts. English et al.[30] have reported $L_T = 20$–40 nm for gold contacts to MoS_2. Note that there is ongoing consideration of where carriers are actually injected at the metal–2D interface, with evidence that top-contacted devices with thinner flakes and contact gating (that is, gate overlap) lead to more edge-dominated injection and thus offer better L_C scalability[82,83]. However, without contact gating, this edge injection behaviour may not hold and thus pure edge-contacted devices may be a more viable solution for aggressively scaled 2D FETs[84].

Doping 2D semiconductors. A comprehensive review of various doping strategies for TMDs has been compiled by Luo and colleagues[85]. In TMDs it is possible to replace both cationic and anionic elements substitutionally by foreign atoms with comparable radii without substantial distortion of the crystal structure of the host material[86]. Cationic elements can be replaced by elements such as niobium[87] and rhenium[88] to achieve p- and n-type doping, respectively (Fig. 4d). However, as the doping has to be introduced during the growth stage, it is difficult to spatially pattern the dopants. Substitutional doping has also been realized by replacing the anions through exposure to plasmas such as carbon[89], nitrogen[90] and so on (Fig. 4e). Although patternable, plasma doping introduces lattice defects, which leads to performance degradation. Additionally, structural incorporation of the dopant in the lattice does not imply dopant activation.

A better doping strategy is SCTD, with which the work function, electron affinity and concentration of the adsorbed or deposited interfacial species determine the type and extent of doping of the underlying 2D channel. SCTD has been demonstrated in several TMD materials, enabling both n- and p-type doping, with varying levels of effectiveness[85]. Doping can also be induced by depositing a sub-stoichiometric insulator such as aluminium oxide[45], amorphous titanium suboxide[54], molybdenum trioxide[79,91,92] or silicon nitride[93] (Fig. 4f). Another approach is ozone or oxygen plasma treatment, which converts the top layer of TMDs to their respective sub-stoichiometric oxides and results in strong p-type doping in the underlying layers[79,91]. In FETs based on multilayer 2D materials, the interlayer space has been exploited for doping via intercalation of foreign ions, atoms and even small molecules, although stability, patternability and fabrication process compatibility are key challenges with this approach. Supplementary Section 5 summarizes some of the most promising doping approaches, their resulting doping type and the corresponding doping concentrations reported for monolayer and multilayer TMDs.

Mobility engineering. The carrier mobility values reported for most 2D materials are substantially lower than their theoretically predicted values, indicating that there is large room for improvement[94]. As a result of the UTB, carrier transport in 2D materials is often not determined by their intrinsic mobility limited by phonon scattering, but by extrinsic effects, including phonon scattering from the dielectrics, Coulomb scattering from the charge impurities, scattering from defects, and surface roughness scattering from the interfaces[95,96]. Point defects are the most important scattering source in TMDs. Owing to the low formation energy of the chalcogen vacancy, a large amount of sulfur vacancies are commonly observed in synthesized MoS_2, which can induce short-range scattering and degrade carrier mobility[97]. Najmaei et al.[98] reported that a self-assembled monolayer can partially repair such vacancies and substantially improve the electron mobility. Ma and Jena[99] predicted that high-κ dielectrics provide effective screening of the charge impurities leading to high Coulomb-limited mobility, but the soft optical phonons in high-κ dielectrics result in low phonon-limited mobility. Selecting moderate-permittivity dielectrics can optimize the carrier mobility in 2D materials. It has been demonstrated that hBN encapsulation of 2D materials reduces scattering from substrate phonons and charged impurities, resulting in higher carrier mobilities[100]. Alternatively, strain can be used for mobility engineering[101].

Scale length. As mentioned earlier, a key motivation for using 2D semiconductors in aggressively scaled devices is their UTB (t_S), which can mitigate so-called short-channel effects, such as drain-induced barrier lowering (DIBL, Box 1). In addition to minimizing the contact dimensions (by improving the contact resistance) and gate-to-contact spacing[102] (including doping), the smallest gate lengths must be achieved by minimizing the electrostatic scale length λ. This scale length represents the competition between the gate and drain potential for control of the channel charge, and a stronger gate-to-channel coupling leads to a desirable, shorter λ. To avoid short-channel effects, the transistor gate length must be at least three to four times larger than λ, which depends on the channel and gate insulator thickness (t_S and t_{OX}), as well as their dielectric constants (ε_S and ε_{OX}). Improvement in λ can be achieved by moving from standard single-gated geometries[82] to dual-gated[24,103], fin[104] and gate-all-around (GAA) geometries[26].

Box 2 | Criteria for the gate dielectric

(1) Yield a gate capacitance of $>3\,\mu F\,cm^{-2}$ to ensure a carrier density of $>10^{13}\,cm^{-2}$ at $V_{GS} < 1\,V$.
(2) Have an electronic structure that, in combination with the semiconductor, allows for small (minimal) thermionic and tunnel gate leakage current $<0.01\,A\,cm^{-2}$ (ref. [194]) as required for LP circuits.
(3) Form an inert interface with the 2D channel material to ensure no reactivity and minimal degradation of carrier mobility (a known issue in silicon technology)[195].
(4) Have low interface and bulk defect/trap density to operate near the ideal SS value of 60 mV dec^{-1} with no detectable hysteresis.
(5) Be compatible with pinhole-free, conformal deposition techniques such as ALD with subnanometre wafer-scale thickness control and low spatial fixed charge variation[196].
(6) Allow for threshold voltage tuning using metal gate work-function engineering to enable NMOS and PMOS without channel doping. This requirement can be relaxed if different 2D materials are used for n-type and p-type channels or if the oxide itself can dope the channel through SCTD[197].
(7) Be suitable for reliable operation for >10 years with a breakdown field of ~10 MV cm^{-1} (ref. [198]).

Dielectric integration. Integration of ultrathin dielectrics is critical to the success of 2D FETs in advanced technologies. Several key criteria need to be satisfied by a candidate gate dielectric stack (transition/buffer layer with suitable high-κ dielectric) to enable a high-performance 2D FET technology (Box 2).

With regards to gate dielectric scaling, there is a need to balance the thickness of the dielectric for minimizing gate leakage current with the push for high gate capacitance for improved gate coupling. According to the IRDS roadmap, the inversion layer thickness must not exceed 0.9 nm (ref. [78]). The inversion layer thickness consists of the EOT and the physical extension of the inversion layer, which amounts to ~0.4 nm, corresponding to the approximate size of the electron orbit[105]. Thus, for an inversion layer thickness of 0.9 nm, an EOT of ~0.5 nm must be achieved with low leakage. For hBN, as one of the most commonly used layered insulators, this corresponds to two atomic monolayers and a physical thickness of ~0.66 nm because of the small permittivity of hBN of ~5. However, this small physical thickness leads to excessive leakage currents that render hBN unsuitable as a gate insulator for 2D FETs at the scaling limit[106]. Instead of hBN, several other insulators for 2D FETs, such as mica[75], HfO_2 (ref. [107]), CaF_2 (ref. [65]) or Bi_2SeO_5 (ref. [76]), could hypothetically offer smaller leakage currents due to their increased physical thickness at the same EOT, provided they can be integrated with the 2D channel as discussed below.

The inert basal planes of 2D semiconductors inhibit the ability to nucleate growth of high-κ dielectrics using standard atomic layer deposition (ALD) processes. Efforts to realize scalable, high-κ dielectrics on top of 2D materials can be broadly classified into four approaches (Fig. 5): surface treatments[23,108,109], ALD process modifications[22,110,111], buffer/seeding layers[65,112–115] and transferred or transformed films[73,76,100,116–118]. For surface treatments, the premise is to generate reactive sites on the otherwise inert basal plane, either by intentionally generating defects or by adding adsorbents. Although it has been suggested that exposing a MoS_2 surface to ozone can lead to a sacrificial oxygen layer on the surface that does not disrupt the MoS_2 crystal and allows for a uniform, pinhole-free Al_2O_3 dielectric using ALD (Fig. 5a)[114], many follow-on reports suggest inconsistencies in this process and reactive oxidation to the 2D crystal[108]. A variety of other surface treatments have been reported, typically in the form of plasma exposure (for example, O_2, H_2 and N_2), but they all tend to exhibit some degree of 2D crystal damage and/or low uniformity.

The second approach to achieving high-κ nucleation is through modification of the ALD process. This is largely related to surface treatments as it involves modification of the precursor choice or inclusion of a plasma precursor step to drive surface functionalization and, ultimately, nucleation. Some of the thinnest high-κ dielectrics so far have been demonstrated using plasma-enhanced ALD (PEALD; HfO_2 down to ~3 nm on MoS_2, Fig. 5b)[111]. However, this process has also been shown to severely damage the topmost 2D layer[110], which may be acceptable in a few-layer film but is a non-starter for monolayers.

Buffer layers can be used to support the nucleation of high-κ dielectrics on 2D channels. However, buffer layers are rarely high-κ and must be as thin and effectual as possible. There has been some success in this regard by using metal oxides formed via the deposition of a thin metal seed layer (for example, electron beam evaporation of Al) followed by its oxidation[45,112], but the evaporation of most metal layers shows damage to the uppermost layers of 2D semiconductors[119]. Others have explored organic films[113], but these tend to suffer from a relatively low electrical permittivity as well as a disordered structure that can lead to large variability. A recent demonstration used a vacuum-phase-deposited molecular crystal monolayer (PTCDA) to achieve an EOT of ~1 nm from an ultrathin high-κ dielectric grown on the seed layer (Fig. 5c)[115]. On the whole, buffer layers pose a scaling challenge as they would need to be simultaneously nanometre-thin, uniform, reliable and as high-κ as possible, although recent PTCDA work does show promise if it can be reproduced more broadly.

The last general approach to realizing a scalable high-κ dielectric on inert 2D surfaces is to use transferred or transformed films. Most common is hBN[116], though other options are emerging, such as MoO_3 (ref. [118]), GaS (ref. [73]) and CaF_2 (ref. [65]). Compelling demonstrations of 'all 2D' transistors have come from these transferred-film approaches[117,120]. Another option is to partially transform the 2D semiconductor into its native high-κ oxide with sub-1-nm EOT (Fig. 5d)[76,107]. This 2D film transformation approach is promising but requires further study to assess the uniformity and yield of the process, which also lacks broad applicability to the diverse range of 2D semiconductors as it would only be compatible with those that are able to be controllably oxidized into a high-quality insulator.

As can be seen, a variety of approaches have been taken to resolve the challenges of integrating a scalable, high-quality dielectric into the gate stack of 2D FETs. Although some of these have shown real promise, the reality is that a viable process will have to be compatible with the demands of a particular technology. It is recommended that continued research efforts consider the uniformity and scalability of proposed processes so that their true utility may be assessed.

Device-to-device variability. The vast majority of the literature on 2D FETs is limited to the demonstration of a few selected devices and does not touch upon the question of yield, that is, the number of devices that achieve comparable performance. Although achieving good device-level metrics such as low contact resistance, high on current and short gate lengths is important for improving system-level performance, device-to-device variation is often the ultimate limiter in transistor scaling and integration. In silicon FinFET technology, variability sources such as work-function variations, fin edge roughness and random dopant fluctuations are well known, monitored and modelled on a wafer scale, contributing to an in-depth understanding that helps to drastically reduce the overall variability[121,122]. In comparison, although 2D FETs will share quite a few of those issues, specific knowledge about variability sources in 2D FETs seems to be fragmentary so far. Recently, a few studies have

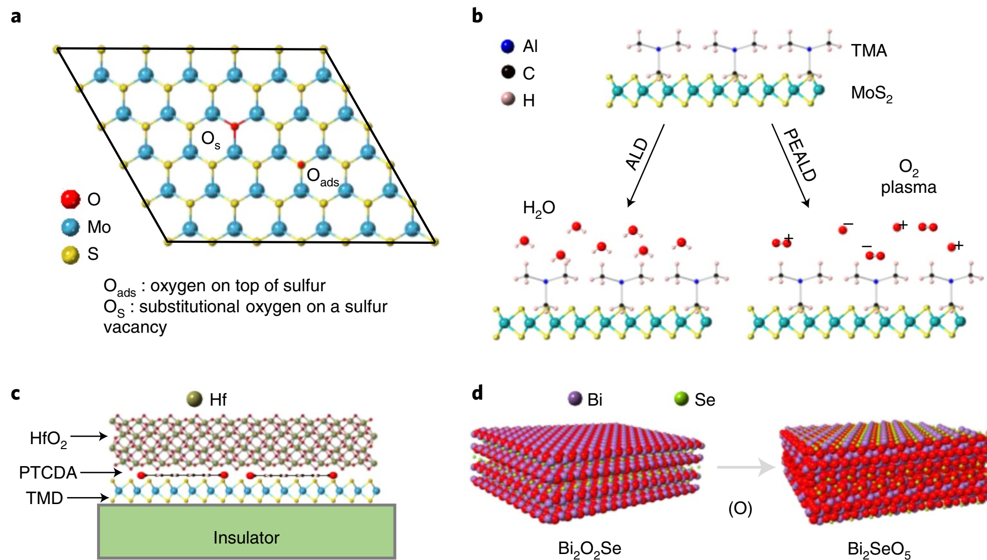


Fig. 5 | Integration of high-κ dielectric on 2D semiconductors. a, Surface treatment with ultraviolet-ozone on MoS_2 (ref. [114]). The 5 × 5 supercell of MoS_2 shown has the most energetically stable adsorption sites for oxygen. **b**, Schematic showing the difference between ALD and PEALD of Al_2O_3 on MoS_2 (ref. [111]). The first step is the same, in which tetramethyl aluminium (TMA) is pulsed into the chamber. However, in the second step, either water vapour (thermal ALD) or O_2 plasma species (PEALD) are introduced. **c**, Use of a molecular crystal seeding layer (PTCDA) to grow ~2 nm HfO_2 on MoS_2 (ref. [115]). **d**, Partial transformation (via oxidation) of semiconducting Bi_2O_2Se to insulating Bi_2SeO_5 with an EOT of ~0.9 nm (ref. [76]).

addressed the variability in 2D FETs at the chip- and wafer-scale level[28,82,103,123–125], as summarized in Supplementary Section 6.

One obvious source of variability in 2D FETs arises from growth defects including the formation of vacancies, multilayer islands and grain boundaries. Vacancies cause unintentional doping and Fermi-level fluctuations within the film and can result in variation in contact resistance[82,126]. Multilayer islands and grain boundaries cause variations arising from quantum confinement effects, local strain fields and defect/substrate-induced charge transfer[127]. Although bilayer islands do not cause V_{TH} variation[28,128], they can cause substantial variation in SS in short-channel devices[128]. Another source of variability comes from physiosorbed and/or chemisorbed impurities at 2D–dielectric interfaces and can cause unintended V_{TH} shift, operational instability, hysteresis and drift in the electrical characteristics[29]. These organic–inorganic interfacial species can originate from the solvents used in the transfer process, lithography or during high-κ dielectric integration. Clean wafer-scale transfer techniques that can minimize cracks, wrinkles and residues can be useful[129,130]. Recently, a wafer-to-wafer bonding and debonding scheme was used for the transfer of WS_2 layers grown on 300 mm wafers in a silicon CMOS[131]. Post-transfer cleaning using plasma can further aid cleaning and restoration of TMDs[20]. The adhesion of the transferred film on the target wafer is also important. Finally, for high-κ dielectric integration, using a gate-first process instead of a gate-last process has been shown to reduce variability[123].

The coefficient of variance and the correlations of important figures of merit that help identify the root causes of the variations are important metrics to quantify device-to-device variability[132]. To decouple device-to-device variation from process-related variability, difference in V_{TH} (obtained from adjacent devices within the same die) can be analysed across multiple dies[103,128]. Similarly, Pelgrom plots can be used to study scaling-induced variations. An encouraging recent study using MoS_2 FETs demonstrated slopes in Pelgrom diagrams similar to those in silicon FinFETs[128]. Assessing temporal variation to study the stability of 2D materials is also crucial[131]. Variation in V_{TH} ($\sigma_{V_{TH}}$) can be used as a benchmarking metric and can be projected for a scaled EOT to account for differences in dielectric environments[28,125], as shown in Supplementary Section 6.

It appears that 2D material defectivity is likely to be the major issue in controlling wafer-scale device variation and performance. For example, according to scanning tunnelling microscopy studies[133] as well as calibration of simulations and mobility data[134,135], the mobility of even the best 2D semiconductors is at present limited by point defect densities on the order of 10^{12} cm^{-2}. The electron mean free path in MoS_2 is only 2–4 nm at room temperature[39]. When defect densities can be lowered below ~10^{11} cm^{-2} at the wafer scale, the mobility will be primarily limited by intrinsic and remote dielectric phonons. In this respect, 2D semiconductors appear more forgiving (to defects) than silicon or III–V semiconductors, in part because the intrinsic mobilities are lower already. Nevertheless, more work is needed to understand how 2D transistor variability and defectivity must be tackled to reach their true potential for future VLSI.

Potential applications for 2D FETs in future VLSI

Two-dimensional FETs offer a broad range of potential VLSI applications, including conventional micro/nanoelectronics, 3D integration, hardware for artificial intelligence, sensing and diffusion barrier replacement for copper interconnects, which we will discuss in the following.

Micro/nanoelectronics. Two-dimensional FETs can be used for standard digital logic, analogue circuits and radiofrequency (RF) electronics, as well as active and passive components in various volatile and non-volatile memory devices including static random-access memory (SRAM), dynamic random-access memory (DRAM) and floating-gate (FG) memory.

For digital logic, the IRDS 2028 node requires a switching delay of ~0.78 ps and switching energy of ~0.47 fJ (ref. [78]). Additionally, the static power must be limited by maintaining I_{OFF} of 10 nA µm^{-1} and 100 pA µm^{-1} for the HP and LP IRDS nodes, respectively. Two-dimensional FETs demonstrate tremendous potential in matching or even outperforming silicon FinFETs in this context[136–138]. Beyond a single device, circuit-level demonstrations of 2D

FETs include a microprocessor[139], an analogue operational amplifier[140] and a SRAM cell[141]. One key consideration for 2D FET-based VLSI is device–circuit co-optimization[142]. For example, the dominant effect of contact resistance can be reduced by reducing interconnect wire dimensions, and the increased power consumption of dual-gated architectures can be reduced by optimizing the back-gate overlap[143].

In addition to helping CMOS logic scaling, 2D transistors can improve memory scaling. Six-transistor (6T) SRAM and its larger version register files are the main memory elements in logic chips. As they are based on logic technology transistors, any scaling, performance and leakage benefits that 2D FETs demonstrate for CMOS would reflect directly on 2D SRAM properties. In fact, SRAM designs based on 2D FETs with a three-tier structure show a substantial increase in memory capacity per unit area for application in future energy-efficient computing systems[144]. Two-dimensional FETs are also very interesting options as DRAM access transistors because they can scale better than silicon FETs while maintaining both low leakage and comparable on current[145]. Various non-volatile memories, such as FG memories, which are key for retaining large amounts of data in electronic products, can use 2D FETs to replace the low-mobility and poor-SS poly-silicon NAND transistors currently in use. However, this will require the growth of 2D channels under a low thermal budget on sidewalls of very high aspect ratio via holes. Good progress with TMD channel growth on oxide sidewalls has been demonstrated[146], but further improvement in transistor performance and scalability is required. Emerging memories such as Fe-FETs, offering better scaling (only one transistor) and high-speed operation (due to the ferroelectric switching mechanism, unlike the slow FG write speed), can also exploit the 2D channel[147]. Beyond memory and logic, 2D FETs can be useful for RF electronics[148], hardware security[149,150], as well as flexible[151] and display[152] electronics.

Three-dimensional integration. Three-dimensional monolithic integration has presented a potential pathway for the future of the semiconducting industry. For the year 2034, table 1 of the IRDS 2020 'More Moore' defines the '07-nm eq node' with a gate length of 12 nm as consisting of four vertically stacked nanosheets with a nanosheet thickness of 5 nm each[78]. In such a way, electrostatic gate control could be preserved while achieving acceptable on-current levels per footprint. The atomically thin nature of 2D materials enables low tier-to-tier signal delay and easier heat dissipation, providing over 150% higher integration density compared to conventional monolithic 3D integration[153]. Such 2D materials also offer good electrostatic screening and high-frequency electric field screening, which are important for 3D integration. Hence, 3D integrated dual-gated WS_2 FETs have demonstrated potential in meeting the requirement of a 3 nm FinFET node[138]. Similarly, high drive current has been achieved in 3D multi-channel MoS_2 FETs[154]. Additionally, ring oscillator circuits based on a GAA MoS_2 FET show potential in outperforming silicon GAA devices at the IMEC 2-nm node[155]. Digital circuit components such as inverters, NAND and NOR components, as well as analogue components such as differential amplifiers, common-source amplifiers and signal mixers, have been demonstrated using 3D monolithic integration of MoS_2 and WSe_2 FETs[156]. Similarly, an all-WSe_2 1T1R resistive RAM cell has demonstrated the potential of 2D materials for 3D embedded memory[157]. Note that monolithic 3D integration of memory and logic is a promising alternative to meet the growing demand for in- and near-memory computing for artificial intelligence and machine learning workloads. Three-dimensional integration can also be used to achieve multifunctional devices in the same chip. For example, a MoS_2 phototransistor array has been integrated on top of a 3D integrated circuit based on a poly-silicon nanowire FET for image sensing applications[158]. The fact that 2D materials can be used to build aggressively scaled transistors, dense memory cells and sensing components provides diverse opportunities for their 3D integration. For these reasons, 2D materials are explicitly mentioned under the rubric 'Technology anchors' subsection of 'Beyond-CMOS as complementary to mainstream CMOS' in the IRDS roadmap.

Interconnect. Two-dimensional materials may also find potential applications in interconnect technology. Copper interconnects are required to become more and more compact at each technology node, inevitably causing an increase in the resistance–capacitance (*RC*) delay in silicon chips. This problem becomes even more severe at ultra-scaled dimensions, because the resistivity of copper rapidly increases with increasing side-wall and grain-boundary scattering[159]. Moreover, it is well known that copper can easily diffuse into the surrounding dielectrics, especially under large electric fields, which necessitates the use of diffusion barriers. A bilayer stack consisting of a nitride (TiN or TaN)-based diffusion barrier and refractory metal (Ta or W)-based liner is usually employed. Because these materials are much more resistive than copper, their thicknesses need to be as thin as possible to achieve overall low line resistances. However, these barrier materials lose their ability to block copper diffusion when they are extremely scaled. Accordingly, a subnanometre barrier solution is urgently desired for ultra-scaled interconnects in the near future. It has been shown by both experiments and simulations[160–163] that 2D materials such as graphene, hBN and various TMDs can be effective diffusion barriers for copper. For example, inserting single-layer MoS_2 between a copper electrode and the underlying dielectric substrate substantially improves device reliability and performance[161]. To realize these 2D materials as potential subnanometre thin barrier solutions for interconnect technology, it is necessary to grow high-quality 2D barriers at BEOL-compatible temperatures. Recent studies have demonstrated the successful conversion of tantalum into a 2D TaS_2 barrier layer at BEOL temperatures, serving as an excellent copper diffusion barrier and adhesion liner to boost the performance of copper interconnects[164,165]. In addition to the diffusion barrier property, the resistivity of the copper/2D-barrier hybrid system has also been critically examined by directly growing graphene on copper nanowires[160] or depositing ultrathin copper films on MoS_2 (ref. [166]) and TaS_2 films[164]. Comparisons of copper resistivity with and without a 2D interface consistently show lower resistivity in scaled copper interconnect devices when 2D interfaces are introduced, which brings substantial value to suppression of the increasing copper resistivity trend in scaled interconnects.

Non-von Neumann computing. Two-dimensional materials also demonstrate potential for post von Neumann computing, such as neuromorphic and biomimetic computing. The physical separation of memory and logic, a key bottleneck of von Neumann computing, can be circumvented through in-memory computing using memristive cross-bar architectures and artificial neural networks[167,168]. In this context, the recent discoveries of 2D memristive devices that exploit phase-transition[169], vacancy or ion migration[170], movements of grain boundaries[171] and dipolar interaction with adsorbed species[172] are promising. Additionally, bio-inspired and biomimetic devices and computing primitives have been demonstrated based on 2D FETs. For example, the auditory cortex of a barn owl can be mimicked using split-gated MoS_2 FETs[25], the visual cortex of the human brain can be emulated using a coplanar multi-gate MoS_2 FET[173] and the escape response of the lobula giant movement detector neuron found in locusts for collision detection can be mimicked using a programmable MoS_2 FET[174]. Furthermore, optically active 2D materials allow for the realization of optoelectronic synapses and smart sensors[167,174,175]. Other neural functionalities such as neurotransmitter release, short- and long-term plasticity, spike-time-dependent plasticity, neural encoding, probabilistic

computing and so on have also been achieved using 2D artificial synapses with substantial energy efficiency[66,170,176,177].

Sensors. Two-dimensional materials, by virtue of their high surface-to-volume ratio, are excellent candidates for sensor applications that exploit surface interactions[178]. For example, a MoS_2-based pH sensor[179], metal-ion pollutant sensors[180] and glucose sensors[181] are some examples of 2D chemical sensors where the target molecules are typically physiosorbed by a van der Waals interaction or chemisorbed into defect sites. Two-dimensional materials can also be decorated with nanoparticles to ensure better electrochemical properties, selectivity and sensitivity[180,181]. Biomolecules such as dopamine, ascorbic acid, uric acid, nucleic acids (DNA and RNA) and various antigens can also be sensed using 2D materials[182]. Such materials are also widely used as gas sensors, which work on the principle of charge transfer between the target molecule and 2D material[77]. These 2D materials also offer potential in thermoelectric applications, where waste heat generated can be converted to electric power to support Internet of things devices[183].

Conclusions

We have examined advances in the growth, fabrication and processing of 2D materials, and outlined the key device parameters that should be used to benchmark the performance of 2D FETs, particularly at scaled device dimensions. We have also identified contact resistance, doping, high-κ dielectric integration and device reliability as the major challenges for scaled 2D FETs. We believe that the direct growth of highly crystalline and defect-free 2D TMDs on existing silicon platforms as well as clean and damage-free wafer-scale transfer from growth substrates are important areas for further investigation to aid the incorporation of 2D FETs into future VLSI technologies. FEOL replacement and/or augmentation requires high-performance 2D FETs, but BEOL integration has relaxed requirements, although it still requires low-temperature growth of 2D materials. Another alternative approach is 3D heterogeneous integration. We have highlighted potential applications of 2D FETs in conventional digital, analogue and RF electronics, as well as non-traditional computing, sensing and various forms of volatile and non-volatile memory. We have also highlighted that 2D materials may be useful as diffusion barriers in aggressively scaled copper interconnects.'

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Author contributions

All authors contributed to the preparation of the manuscript.

Competing interests

The authors declare no competing interests.

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Supplementary information

Transistors based on two-dimensional materials for future integrated circuits

In the format provided by the authors and unedited

Supporting Information

Transistors based on two-dimensional materials for future integrated circuits

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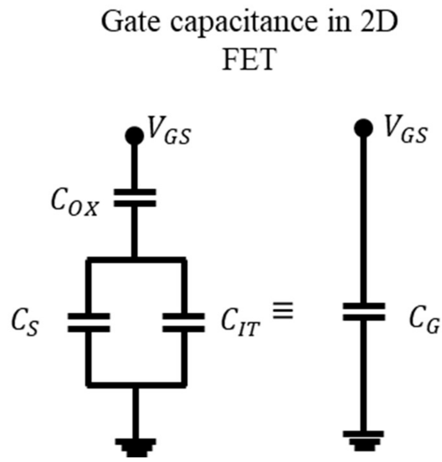
Supporting Information 1

$$n_S = C_G(V_{GS} - V_{TH} - V_{DS}/2)/q \quad [S1]$$

$$C_G = \frac{C_{OX}(C_S + C_{IT})}{C_{OX} + C_S + C_{IT}} \quad [S2]$$

C_G, C_S, and C_{IT} are, respectively, the gate, channel, and interface trap capacitances per unit area.



While most reports assume that for ultrathin body (UTB) 2D FETs in inversion, $C_G \approx C_{OX}$, where C_{OX}, is the oxide capacitance per unit area, this approximation may not hold if the channel material has low density of states and/or large interface trap capacitance (C_{IT}). Furthermore, C_{OX} is estimated using ${}^{\varepsilon_{ox}}/_{t_{ox}}$, where t_{ox} and ε_{ox} are, respectively, the thickness and dielectric constants of the gate oxide noting that there are often variations in ε_{ox}, particularly from novel dielectrics such as hBN as well as atomic layer deposition (ALD) grown Al_2O_3, HfO_2 etc. Therefore, C_G *versus* V_{GS} measurement is recommended for a more accurate evaluation of the gate capacitance.

Supporting Information 2

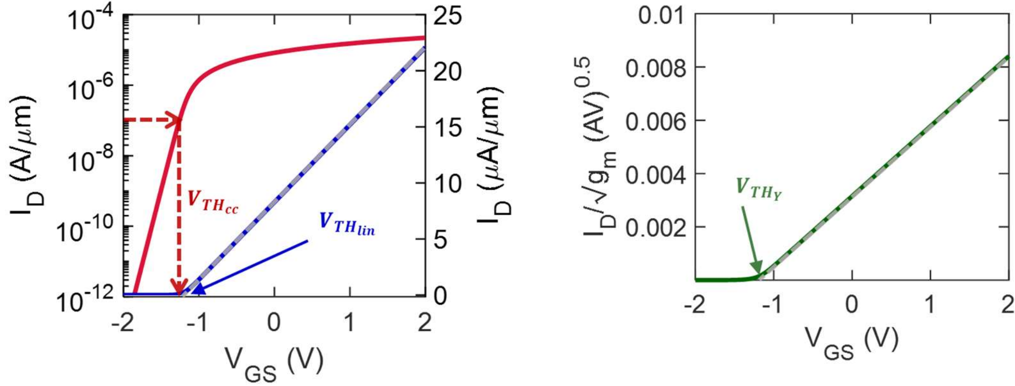


Figure S1: *Illustration of extraction of threshold voltage for 2D FETs*

$$Y = \frac{I_{DS}}{\sqrt{g_m}} = \left(V_{GS} - V_{TH_Y}\right)\sqrt{\mu_Y W C_G V_{DS}} \qquad [S3]$$

$$g_m = \frac{dI_{DS}}{dV_{GS}}; \quad \mu_{g_m} = \frac{g_{m,max} L}{W C_G V_{DS}} \qquad [S4]$$

μ_{g_m} is extracted using the peak value of transconductance (Eq. S4). Note that μ_{g_m} can be prone to error especially when R_C shows a strong V_{GS} dependence. It is commonly believed that μ_{g_m} is underestimated for 2D FETs due to contribution from R_C, Nasr *et al.* [1] have shown that overestimation of μ_{g_m} is equally likely in commonly used 2D FET geometries with back-gated contacts.

μ_Y is extracted using the slope of Y-function *versus* $V_{GS} - V_{TH_Y}$ (Eq. S3)

μ_{TLM} is extracted using the TLM test structures (Fig. 1d), which have a sequence of channels of identical width, with contacts of increasing separation, L [2]. In units normalized by width (e.g. Ω·µm) the TLM equation is:

$$R_T = LR_{SH} + 2R_C; \quad R_{SH} = \frac{L}{qn_S \mu_{TLM}} \qquad [S5]$$

Where R_T is the total resistance and R_{SH} is the sheet resistance of the 2D channel. R_{SH} and $2R_C$

are extracted as the slope and y-intercept of a linear fit to the measured R_T versus L data (Fig. 1g). μ_{TLM} is also referred to as the effective mobility in the literature. In reporting R_C, R_{SH}, and μ_{TLM}, it is important to give their extraction errors from the least squares fit, e.g. the 95% confidence interval. Additional error can arise from n_S estimation, e.g. due to measurement hysteresis. We recommend the following steps:

1. Measure R_T of channels with a range of L from "short" (dominated by $2R_C$) to "long" (dominated by LR_{SH}).
2. Use low V_{DS} (linear region) and subtract any resistance contribution from metal lines, if needed.
3. Group the $R_T(L)$ at the same n_S not same V_{GS}, accounting for V_{TH} variation or hysteresis among channels.
4. Use least squares fit to extract the y-intercept ($2R_C$) and slope (R_{SH}), reporting them with the respective errors.

Subthreshold slope (SS) is given by Eq. S5, and for fully-depleted UTB 2D FETs, $C_S \approx 0$. Hence the SS is dominated by C_{IT}.

$$SS = m\frac{k_BT}{q}ln10\left(\frac{mV}{decade}\right); \qquad m = \left(1 + \frac{C_S + C_{IT}}{C_{OX}}\right); \qquad C_{IT} = q^2D_{IT} \qquad [S6]$$

Supporting Information 3

Velocity saturation in semiconductors has been studied since the 1950s [3], and researchers have found that v_{sat} scales as $\left({E_{op}}/{m^*}\right)^{1/2}$, where E_{op} is the optical phonon energy that dominates scattering (~60 meV in Si) and m^* is the electron or hole effective mass [4]. This observation carries over to 2D materials [5, 6], where in graphene v_{sat} reaches up to ~6×10^7 cm/s due to its large $E_{op} \approx$ 180 meV [7]. On the other hand, 2D semiconductors like MoS_2 and WS_2 have lower E_{op} (~40 meV) and heavier effective masses than Si. In addition, due to the 2D material thinness, scattering with remote phonons [8] of the gate insulator is likely to put additional limits on v_{sat}. Note that the peak intrinsic frequency (f_T) of a transistor also depends on v_{SAT} following, $f_T \approx {v_{sat}}/{2\pi L}$ [4]. Even in truly nanoscale transistors, where velocity overshoot or ballistic effects could dominate, a subset of charge carriers are ultimately limited by velocity saturation effects [9]. Initial reports found $v_{sat} \approx 3\times10^6$ cm/s in MoS_2 [6, 10]. However, since these measurements were carried out in a high-current DC regime, where self-heating (SH) and charge trapping are difficult to rule out, v_{sat} is expected to be underestimated. More recent measurement using nanosecond-range pulses estimated $v_{sat} \approx 6\times10^6$ cm/s for MoS_2 on SiO_2 [11], reducing SH and hot carrier capture by deep oxide traps.

Supporting Information 4

Self-heating (SH) is often present during high-field and high-current measurement of 2D FETs. The temperature rise due to SH of an SOI-like transistor can be estimated with a simple model, $\Delta T = PR_{TH}$, where the input power is $P = I_D V_{DS}$, and the thermal resistance $R_{TH} \approx \left(TBR + {t_{OX}}/{k_{OX}}\right)/(WL)$, where TBR ≈ 6 x 10^{-8} m^2K/W is the thermal boundary resistance between the 2D channel and the underlying insulator [12], t_{OX} is the thickness and k_{OX} (~1.4 $Wm^{-1}K^{-1}$ near room temperature) is the thermal conductivity of the underlying insulator (SiO_2). This simple model is useful for a quick estimate in micron-scale transistors, while more extensive models can include the thermal resistance of the substrate beneath the SiO_2 [12] and heat sinking to the device contacts [6, 13], which can be important in sub-micron transistors.

Supporting Information 5

Table S1: Summary of doping strategies for 2D materials						
	2D Material	#Layer	Dopant	Doping Type	Carrier concentration	Reference
Substitutional Doping	MoS_2	ML	Nb	*p*	1.8×10^{14}	[14]
		ML	P	*p*	10^{10} - 10^{12}	[15]
		1L	Re	*n*	5.5×10^{12}	[16]
	WS_2	1L,ML	N	*p*	3.8×10^{12}	[17]
		ML	Cl	*n*	6×10^{11}	[18]
	WSe_2	1L	V	*p*	4.8×10^{12}	[19]
	$MoSe_2$	1L	W	*p*	4×10^{11}	[20]
Surface charge transfer doping (SCTD)	MoS_2	ML	$AuCl_3$	*p*	5×10^{13}	[21]
		1L	TiO_x	*n*	7.4×10^{12}	[22]
		1L	AlO_x	*n*	2.0×10^{13}	[23]
		ML	PVA	*n*	8×10^{12}	[24]
		ML	BV	*n*	1.2×10^{13}	[25]
		ML	K	*n*	1×10^{13}	[26]
		ML	MoO_x	*p*	2.5×10^{13}	[27]
	WS_2	ML	WO_x	*p*	1.5×10^{13}	[27]
	WSe_2	1L	NO_2	*p*	2.2×10^{12}	[28]
		ML	MoO_3	*p*	2×10^{13}	[29]
		ML	WO_x	*p*	2.6×10^{12}	[30]
		ML	K	*n*	2.5×10^{12}	[26]
		1L,ML	SiN_x	*n*	9.5×10^{13}	[31]
		ML	WO_x	*p*	1.5×10^{13}	[27]
	$MoTe_2$	ML	O_2	*p*	5×10^{12}	[32]
		ML	BV	*n*	5.2×10^{12}	[32]

1L: One Layer; ML: Multilayer

Supporting Information 6

Device-to-Device Variation Studies							
Ref	[33]	[34]	[35]	[36]	[37]	[38]	[37]
2D Material	MoS_2	MoS_2	MoS_2	MoS_2	MoS_2	WS_2	WS_2
Growth Method	CVD	MOCVD	CVD	CVD	MOCVD	MOCVD	MOCVD
Temperature	650 ˚C	850 ˚C	850 ˚C	650 ˚C	1000 ˚C	750 ˚C	1000 ˚C
Growth Wafer	1 cm^2 SiO_2	2” Sapphire	1 cm^2 SiO_2	2” Sapphire	2” Sapphire	12” SiO_2	2” Sapphire
Transfer	✓	✓	×	×	✓	×	✓
Gate Dielectric	30 nm Al_2O_3(B)	50 nm SiO_2, 16/8/4 nm HfO_2(B)	30 nm SiO_2(B)	30 nm HfO_2(T)	50 nm Al_2O_3(B)	10 nm HfO_2(T), 50 nm SiO_2(B)	50 nm Al_2O_3(B)
Channel Length	2 µm - 4 µm	29 nm - 10 µm	4 µm - 9 µm	10 µm - 100 µm	100 nm - 5 µm	150 nm (T) 220 nm (B)	100 nm - 5 µm
Number of Devices	200	1300	200	150	230	≈ 170	160
σ_{Vt}	0.17 V	44 mV	1.05 V	0.1 V	0.8 V	-	0.8 V
Scaled σ_{Vt} (EOT=0.9 nm)	11 mV	20 mV	33 mV	19 mV	33 mV	63 mV (T) 36 mV (B)	33 mV

B: Back-gate; T:Top-gate

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