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Unveiling the Effect of Superlattice Interfaces and Intermixing on Phase Change Memory Performance

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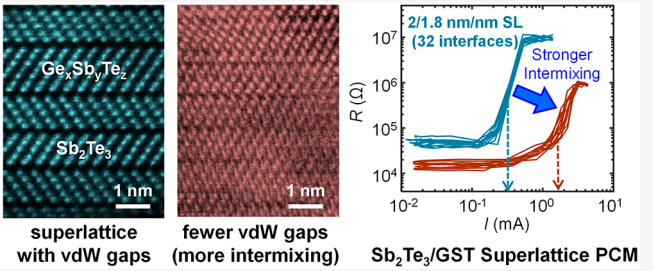
ABSTRACT: Superlattice (SL) phase change materials have shown promise to reduce the switching current and resistance drift of phase change memory (PCM). However, the effects of internal SL interfaces and intermixing on PCM performance remain unexplored, although these are essential to understand and ensure reliable memory operation. Here, using nanometer-thin layers of $Ge_2Sb_2Te_5$ and Sb_2Te_3 in SL-PCM, we uncover that both switching current density (J_{reset}) and resistance drift coefficient (ν) decrease as the SL period thickness is reduced (i.e., higher interface density); however, interface intermixing within the SL increases both. The signatures of distinct versus intermixed interfaces also show up in transmission electron microscopy, X-ray diffraction, and thermal conductivity measurements of our SL films. Combining the lessons learned, we simultaneously achieve low $J_{reset} \approx 3-4$ MA/cm^2 and ultralow $\nu \approx 0.002$ in mushroom-cell SL-PCM with ∼110 nm bottom contact diameter, thus advancing SL-PCM technology for high-density storage and neuromorphic applications.



KEYWORDS: *$Sb_2Te_3/Ge_2Sb_2Te_5$ superlattice, superlattice interface, superlattice intermixing, phase-change memory, switching current density, resistance drift*

In the early part of the 21st century, computing systems have been reaching fundamental limits with conventional materials and conventional layouts which separate memory and computing.[1] To overcome these challenges, phase change memory (PCM) technology based on chalcogenides like $Ge_2Sb_2Te_5$ (GST) holds great promise for both data storage and neuromorphic computing.[1−5] Thermally driven phase transitions in PCM are achieved using electrical pulses to induce crystallization (low resistance state) and melt-quenched amorphization (high resistance state) of the phase change chalcogenide materials.[2,3]

PCM based on GST is a mature data storage technology,[6] bridging the performance gap between existing memory technologies such as flash and dynamic random-access memory, while providing faster speed, larger memory window, and longer write endurance than flash.[3] These attributes of PCM, along with its potential for multilevel memory are useful for data storage and neuromorphic computing.[7,8] However, PCM based on traditional chalcogenides like GST requires relatively large power consumption and suffers from resistance drift, which pose challenges for its widespread adoption in brain-inspired computing.[9,10]

Recently, superlattice (SL) phase change materials with ultrathin alternating layers (e.g., $TiTe_2/Sb_2Te_3$, $GeTe/Sb_2Te_3$, or $GeSb_2Te_4/Sb_2Te_3$) have been reported to lower the switching current density (J_{reset}), resistance drift coefficient (ν), and switching time in PCM.[7,11−15] Low cross-plane thermal conductivity and high cross-plane electrical resistivity of the SL films generate electro-thermal confinement in SL-PCM, driving the energy-efficiency in such devices.[14,16−18] The electro-thermal properties of the SL materials stem from the van der Waals (vdW)-like interfaces within the SL,[17−20] which have also been studied in other material systems;[21,22] the vdW-like interfaces are qualitatively similar but weaker than in covalently bonded SLs[23] such as SiGe. Thus, SL interfaces, in particular their interface density and their intermixing (i.e., loss of vdW-like gaps, stacking faults, and disordering),[24] can play a key role in the SL-PCM device performance.

However, SLs have not been studied with the well-known phase change material $Ge_2Sb_2Te_5$ (GST), and the correlation between the SL interfaces (i.e., interface density, intermixing) and memory performance (J_{reset} and ν) also remain unexplored

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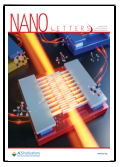

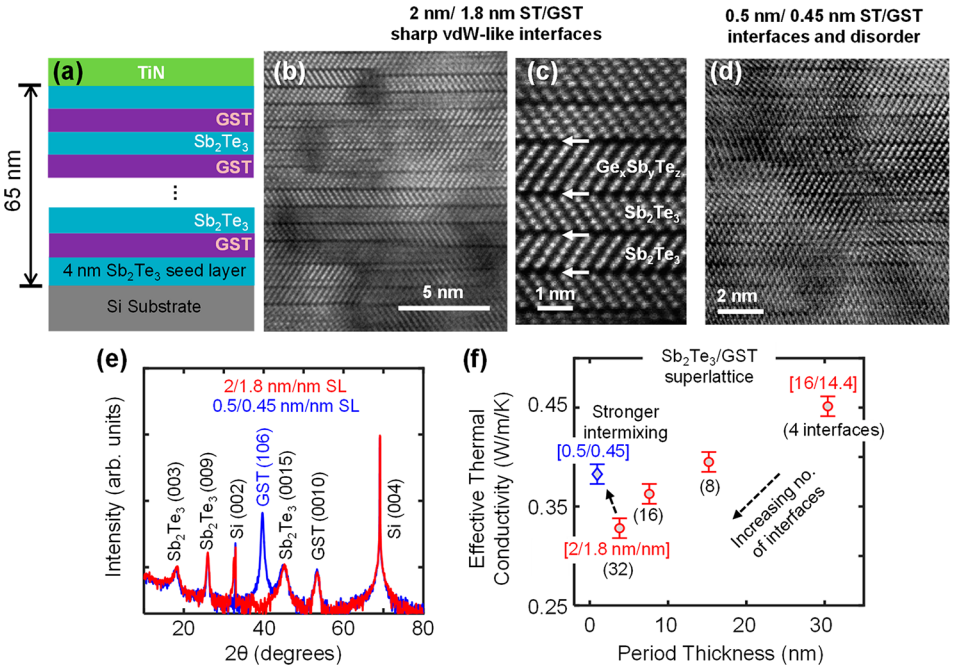

Figure 1. Material and thermal characterization of ST/GST superlattices. (a) Schematic of our SL stacks with alternating Sb_2Te_3 and $Ge_2Sb_2Te_5$ up to ~65 nm total thickness including the ~4 nm ST seed. (b) High-angle annular dark-field scanning transmission electron microscopy (STEM) cross sections of our 2/1.8 nm/nm ST/GST SL showing sharp interfaces and vdW-like gaps parallel to the substrate. (c) Zoomed-in higher resolution version of the same STEM. (d) High-resolution STEM cross-section of a 0.5/0.45 nm/nm ST/GST SL (with layers smaller than the unit block thicknesses of ST and GST) reveals loss of vdW-like interfaces, decreased structural order, and stacking faults representing an intermixed SL. (e) X-ray diffraction spectra of the same SLs as in (b,d), showing polycrystallinity of the as-deposited films. For the intermixed SL (0.5/0.45 nm/nm), non-out-of-plane GST peaks appear. (f) Cross-plane thermal conductivity of our SLs (all ~65 nm thick) with varying ST/GST period thickness at room temperature. Thermal conductivity decreases when more interfaces are present, except for the thinnest layers which show interfacial intermixing, that is, loss of vdW-like interfaces due to the formation of additional grains and disordering within the SL.

and are the subjects of this study. We find that both switching current and resistance drift in SL-PCM devices can be controlled with the number of internal SL interfaces, as well as the quality of these interfaces. Material characterization and thermal conductivity measurements of our SLs further support this important correlation between the memory device characteristics and the SL interface properties. Utilizing these, we simultaneously achieve low J_{reset} and ν in our SL-PCM devices, maintaining these attributes from room temperature up to 105 °C, and even after extensive electrical cycling.

Figure 1a shows a schematic of our sputtered SL on a silicon (Si) substrate with alternating Sb_2Te_3 (ST) and $Ge_2Sb_2Te_5$ (GST) layers deposited at 180 °C (~65 nm in total thickness including an ~4 nm ST seed layer). The seed Sb_2Te_3 layer is deposited at room temperature (RT) and annealed to 180 °C, followed by the sputter deposition of the subsequent GST and ST layers at 180 °C (see Supporting Information Section 1 for details). All superlattices were capped in situ at RT with ~10 nm sputtered TiN to avoid oxidation. To understand the effect of the internal interfaces, we fabricated ST/GST superlattices of varying period thicknesses (i.e., 1/number of interfaces) but keeping the total stack thickness fixed (~65 nm). Figure 1b,c shows high-resolution scanning transmission electron microscope (STEM) images of a 2/1.8 nm/nm ST/GST superlattice, revealing atomically sharp interfaces separated by van der Waals (vdW)-like gaps, representing a good quality superlattice. In contrast, an ST/GST superlattice deliberately chosen with sub-nanometer thin period (0.5/0.45 nm/nm in Figure 1d) shows stronger intermixing within layers, that is, loss of vdW-like gaps, and more stacking faults or disordering. We note that for this superlattice, the individual ST/GST layers are smaller than the unit block thicknesses of ST (~1 nm) and GST (~1.8 nm); therefore, a greater degree of intermixing is expected. X-ray diffraction (XRD) spectra for the as deposited superlattices (Figure 1e) on a Si substrate (with native amorphous SiO_2) confirm their polycrystallinity, while a non-out-of-plane GST peak appears in the 0.5/0.45 nm/nm SL spectra, referring to the formation of additional randomly oriented grains[24] and thus additional disorder within the SL.

We measured the effective cross-plane thermal conductivity (k_{eff}) of our superlattices (Figure 1f) with varying period thickness using a time domain thermoreflectance (TDTR) technique described in detail elsewhere.[17,25] Our measured k_{eff} of the ST/GST superlattices decreases with increasing number of interfaces, that is, with decreasing period thickness from 16/14.4 nm/nm (4 interfaces) to 2/1.8 nm/nm (32 interfaces). A minimum $k_{eff} \approx 0.33 \pm 0.01$ $Wm^{-1}K^{-1}$ is measured for the 2/1.8 nm/nm stack. (Note here k_{eff} includes the 10 nm TiN capping and 70 nm Pt transducer on top, see Supporting Information Figure S1.) The inverse relationship between k_{eff} and the number of interfaces is attributed to the vdW-like gaps impeding cross-plane thermal transport.[16,17] However, when the period thickness is reduced such the individual ST and GST layers are below their unit block thicknesses, k_{eff} increases (here for 0.5/0.45 nm/nm SL) due to stronger intermixing, that is, loss of vdW-like gaps within the SL, also evident from our STEM (Figure 1d). We further note that the measured thermal conductivity of the more intermixed

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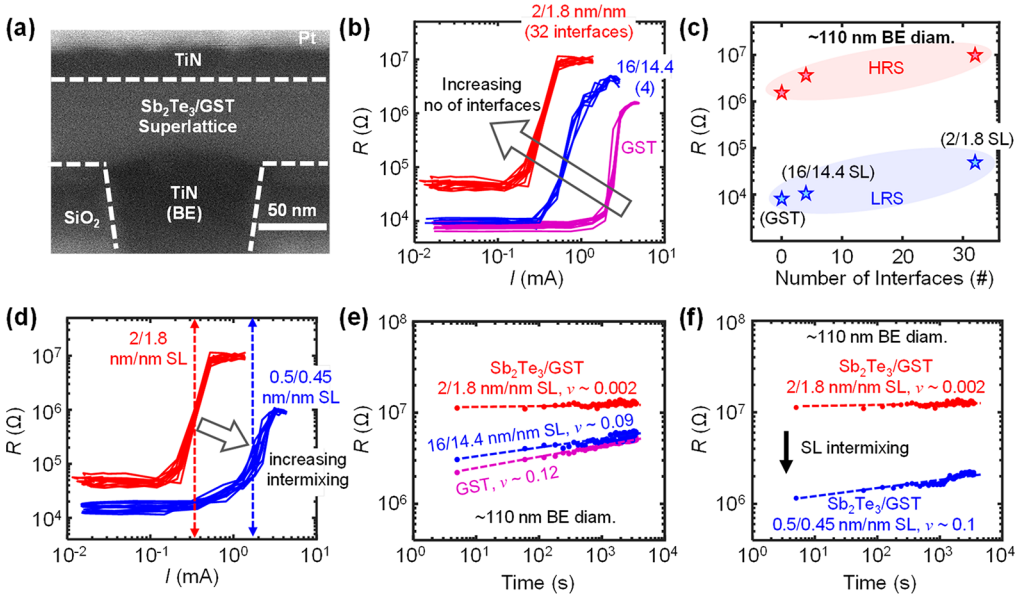

Figure 2. SL-PCM device measurements and the effect of interfaces and intermixing. (a) Scanning electron microscope cross-section of an ST/GST mushroom cell with ∼110 nm bottom electrode (BE) diameter. (b) Resistance (R) versus current (I) measurements comparing well-cycled SL-PCMs with varying SL interfaces (e.g., 32 interfaces for 2/1.8 nm/nm SL and 4 interfaces for 16/14.4 nm/nm SL) versus well-cycled GST-PCM (no internal interface). Ten different cycles are shown for each device type. (c) Effect of the number of interfaces on the average lowest resistance states (LRS, blue) and the average highest resistance states (HRS, red) of SL-PCMs and GST (zero interfaces). (d) R versus I of SL-PCMs showing increased I_{reset} for 0.5/0.45 nm/nm ST/GST (intermixed with rougher interfaces, see Figure 1d) compared to 2/1.8 nm/nm ST/GST (better quality interfaces). Vertical dashed lines represent I_{reset} defined by the current (I) required for at least a ∼10× change in R. (e) HRS versus time for SL-PCMs with varying number of interfaces and for control GST-PCM. Dashed lines are fit using $R \propto t^{\nu}$, where t is time and ν is the resistance drift coefficient. ν decreases with increasing number of SL interfaces. (f) Similar HRS drift measurement of PCM with intermixed SL (0.5/0.45 nm/nm) reveals a significant increase in ν compared to SL-PCM with sharper interfaces (2/1.8 nm/nm ST/GST). All PCM devices have a BE diameter of ∼110 nm, the SL and GST films are ∼65 nm thick, and all measurements are at room temperature.

SL is still lower than the thermal conductivity of polycrystalline GST.[17] A similar phenomenon has been reported for SiGe superlattices versus bulk SiGe, attributed to the combined effects of interface (roughness) and internal (alloy) scattering.[23,26] Thus, material and thermal properties of SLs are controlled by the number of interfaces and their degree of intermixing, which can play a crucial role in controlling the SL-PCM performance as we will explore below.

Figure 2a shows the scanning electron microscope cross-section of a fabricated mushroom-cell SL-PCM device with 2/1.8 nm/nm ST/GST superlattice between a TiN bottom electrode (BE) of ∼110 nm diameter and a top electrode (TiN/Pt). We also fabricated control PCM devices with the same dimensions, but only with GST instead of the ST/GST stack. The device fabrication process is detailed in Supporting Information Section 2. We programmed the SL-PCM devices using 1/20/300 ns and 1/20/1 ns rise/width/fall pulses for set and reset, respectively. The PCM devices with only GST needed a longer set fall time (500 ns) for reliable switching, and the electrical measurement setup is described in detail elsewhere.[7,27]

Figure 2b compares resistance (R) versus current (I) measurements of well-cycled SL-PCM and control GST devices (cycled >1000 times) with same total film thickness (∼65 nm) and BE diameter (here ∼110 nm). The reset current (I_{reset}) in 2/1.8 nm/nm SL with 32 internal interfaces decreases compared to 16/14.4 nm SL with 4 internal interfaces and with GST-PCM (with no internal interface), revealing an interface-controlled switching current in SL-PCM devices. Figure 2b shows that an ∼7−8× reduction in I_{reset} is achieved in 2/1.8 nm/nm SL-PCM (∼0.35 mA) compared to a control GST device (∼2.5 mA) of same BE diameter. The SL-PCM with more internal SL interfaces show lower I_{reset} due to improved electro-thermal confinement originating from the higher number of vdW-like interfaces[16,18,28] that are maintained during device switching.[16] Figure 2c reflects that the lowest resistance state (LRS) and the highest resistance states (HRS) of the devices also increase with more SL interfaces pointing to higher cross-plane electrical resistivity within the SL due to additional vdW-like gaps.[16,17] Figure 2c also shows that a resistance on/off ratio of ∼100 is maintained for the SL-PCM (and GST PCM) regardless of the number of interfaces.

Figure 2d reveals a larger I_{reset} in the more intermixed 0.5/0.45 nm/nm SL-PCM compared to 2/1.8 nm/nm SL-PCM. In fact, I_{reset} in 0.5/0.45 nm/nm SL-PCM is nearly comparable to that in our control GST PCM (with no internal interfaces) highlighting the detrimental effect of SL intermixing and rough interfaces on the switching current (and voltage, see Supporting Information Figure S2) of SL-PCM. We also find a lower LRS in the more intermixed SL-PCM device (Figure 2d) that can be explained by a lower cross-plane electrical resistivity resulting from the lack of sharp vdW-like interfaces in an intermixed SL.[17,29]

Figure 2e and Supporting Information Figure S3 show a clear trend of decreasing resistance drift coefficient (ν) of the highest resistance states from GST (no internal interfaces) to 16/14.4 nm/nm SL (4 interfaces) to 2/1.8 nm/nm ST/GST SL (32 interfaces). Extracted $\nu \approx 0.002$ for 2/1.8 nm/nm SL-PCM is ∼50× lower compared to our control GST PCM ($\nu \approx 0.11$), promising for multibit high-density PCM. On the other hand, deliberate intermixing within an SL (here 0.5/0.45 nm/nm) increases ν, as seen in Figure 2f. These findings highlight

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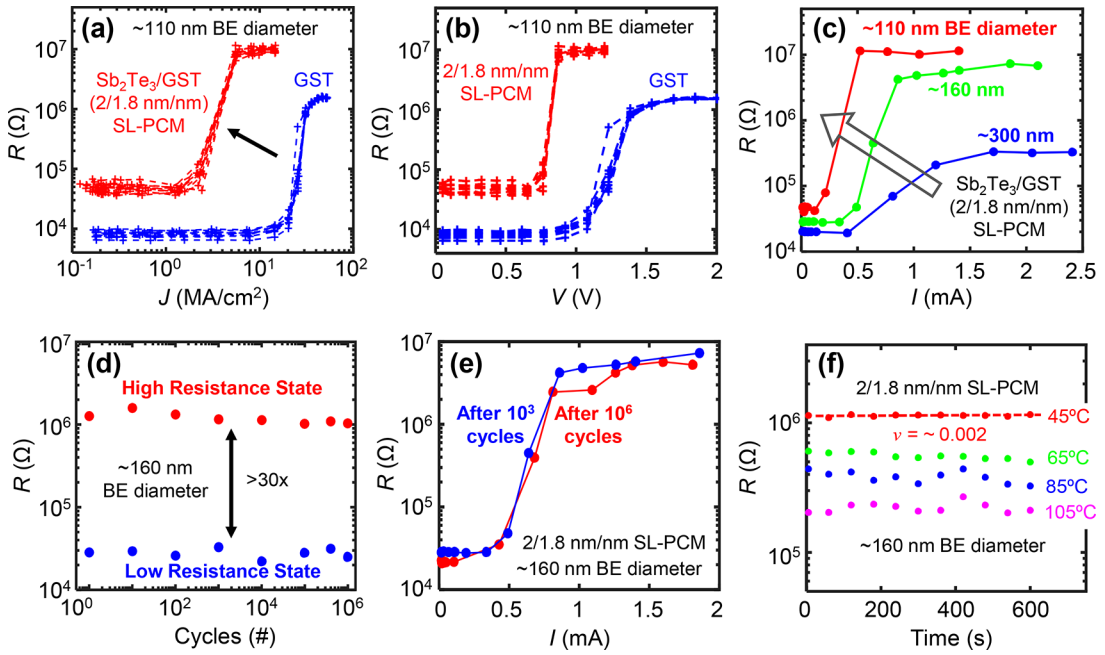

Figure 3. Low switching current density, scalability, robustness, and temperature stability of 2/1.8 nm/nm Sb_2Te_3 (ST) /GST SL-PCM. (a) Resistance (R) versus current density (J) showing a significant improvement of reset current density (J_{reset}) in ST/GST SL-PCM versus GST PCM (here both devices have a BE diameter of ~110 nm). (b) R versus voltage (V) for ST/GST SL-PCM and control GST devices with ~110 nm BE diameter. (c) Scalability of I_{reset} with BE diameter for SL-PCM devices. (d) Resistance on/off ratio >30× maintained during >10^6 switching cycles in an SL-PCM device (~160 nm BE diameter) measured using 1 V; 1/20/1 ns (rise/width/fall time) reset and 1 V; 1/20/300 ns set pulses. (e) R versus I after 10^3 (in blue) and 10^6 (in red) switching cycles showing that low I_{reset} and the resistance on/off ratio (~100×) are maintained in our ST/GST 2/1.8 nm/nm SL-PCM devices even after extensive electrical cycling. (f) R versus time measured in a 2/1.8 nm/nm ST/GST SL-PCM (~160 nm BE diameter) at different temperatures (up to 105 °C), demonstrating that low resistance drift coefficient (ν) is retained even at higher temperatures.

the importance of the internal vdW-like interfaces in lowering ν.

Such correlation between SL-PCM key performance indicators (switching current and resistance drift coefficient) and SL interface property (number of internal interface and degree of intermixing) can open the pathway toward low-power data storage using SL-PCM technology. Figure 3a displays that the estimated reset current density (J_{reset}) of 2/1.8 nm/nm Sb_2Te_3/GST SL-PCM is ~3−4 MA/cm^2, an ~7−8× reduction compared to control GST PCM (20−25 MA/cm^2). Figure 3b compares the R versus voltage (V) for the same SL-PCM with control GST devices with the same BE diameter (~110 nm). Estimated reset power (from R versus I in Figure 2b and R versus V in Figure 3b) for our 2/1.8 nm/nm ST/GST SL-PCM device is ~0.28 mW, over an order of magnitude improvement compared to the control GST PCM (~3.38 mW) with the same BE diameter. Figure 3c displays the scalability of I_{reset} with BE diameter (here from 300 nm down to ~110 nm), for our SL-PCM devices. R versus V also scales with BE diameter (Supporting Information Figure S4), thus confirming the scalability of switching power with BE diameter in our SL-PCM technology, important for future ultrascaled devices.

Figure 3d shows the cyclability of a 2/1.8 nm/nm SL-PCM device with ~160 nm BE diameter for >10^6 switching cycles, maintaining a resistance on/off ratio >30×. The low I_{reset} (and switching voltage V_{reset}; see Supporting Information Figure S5) and resistance on/off ratio are maintained even after extensive electrical cycling, demonstrating the robustness of our low power SL-PCM devices (Figure 3e). We also explored the temperature stability of the resistance drift for our SL-PCM devices. Figure 3f reveals that the low resistance drift measured in our SL-PCM is maintained at higher temperature (up to 105 °C for a 2/1.8 nm/nm SL-PCM with ~160 nm BE diameter).

Thus, by controlling the number of SL interfaces and limiting intermixing, we simultaneously achieve $J_{reset} \approx 3.5$ MA/cm^2 and $\nu \approx 0.002$ in GST/ST SL-PCM, approaching the best corner on the PCM technology benchmarking plot in Figure 4. However, significantly higher J_{reset} and ν is observed for SL-PCM devices with fewer SL interfaces and in our control GST-PCM (without internal interfaces). This establishes the importance of SL material optimization and interface control (e.g., choice of SL material layers, their period thickness, suitable deposition conditions, and methods) for next-generation, low-power and high-density SL-PCM technology. The benchmarking plot in Figure 4 also highlights the advantages of superlattice-based PCM technology compared to other existing PCM technologies[9,30−36,38,39] in reducing PCM switching current and resistance drift simultaneously.

In summary, we demonstrated that both switching current and resistance drift in Sb_2Te_3/GST superlattice PCM are intimately tied with the number and degree of intermixing of the internal SL interfaces. The switching current density (J_{reset}) and resistance drift coefficient (ν) decrease with increasing number of SL interfaces, while a higher degree of intermixing and imperfections within the SL layers increase both key performance indicators in an SL-PCM device. By controlling the number of SL interfaces as well as preserving the interface quality, we demonstrated low J_{reset} (≈ 3−4 MA/cm^2) and ν (≈ 0.002) simultaneously in the same SL-PCM device (based on a superlattice of Sb_2Te_3/GST 2/1.8 nm/nm) with bottom electrode diameter down to 110 nm. The low J_{reset} and ν are

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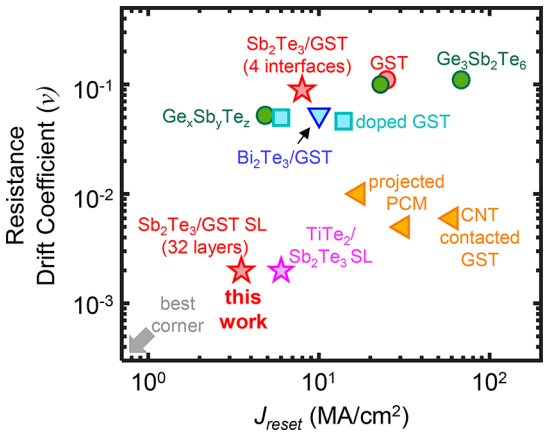

Figure 4. Benchmarking of reset current density (J_{reset}) and resistance drift coefficient (ν) for various PCM technologies. Simultaneously low J_{reset} and low ν are achieved in our SL-PCM (with 2/1.8 nm/nm Sb_2Te_3/GST and 32 internal interfaces), approaching the most desirable corner on this plot, compared to other PCM technologies from the literature.[9,11,30−37] (The best corner is defined by the region where both J_{reset} and ν are simultaneously low.) SL-PCMs and control GST in this work are shown with red stars and red circle, respectively. Note, GST represents $Ge_2Sb_2Te_5$ stoichiometry.

retained even after 10^6 switching cycles and at high temperature (105 °C), respectively, showing promise for low-power, high-density stable PCM operation. These results provide key insights toward new superlattice material design and optimization for this novel SL-PCM technology.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c01869.

Superlattice (SL) film deposition; fabrication process of SL phase change memory device; additional figures showing schematic for thermal measurements; additional device data (PDF)

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Author Contributions

A.I.K and E.P. conceived the idea. A.I.K and C.P. designed the experiments. A.I.K fabricated the devices with help from X.W. and H.K. A.I.K and X.W. performed the electrical measurements. P.R. helped with temperature-dependent measurements with support from K.S. Thermal measurements were carried out by C.P. and H.K. (with inputs from M.A and K.E.G.). STEM and XRD were performed by B.W. and K.K (with support from I.O. and Z.L.). M.T. and C.P. performed the SEM. A.I.K. and E.P wrote the manuscript with inputs from H.-S.P.W. All authors discussed the results and edited the manuscript.

Author Contributions

○X.W. and C.P. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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Supporting Information

Unveiling the Effect of Superlattice Interfaces and Intermixing on Phase Change Memory Performance

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Section 1. Superlattice Film Deposition Process

The phase change superlattices ($Sb_2Te_3/Ge_2Sb_2Te_5$) were sputtered using a AJA ATC-1800 magnetron sputtering system. For material characterization and thermal measurements in Figure 1, we deposited the superlattice (SL) films on Si substrate with high resistivity. Prior to the sputter deposition, the Si substrate was in situ cleaned by Ar ion etching [30 standard cubic centimeters per minute (sccm) Ar flow, 50 W radio-frequency (RF) bias for 600 seconds] to remove any native oxide and clean the substrate. Then we deposited a ~4 nm thick Sb_2Te_3 seed layer at room temperature. Then, the seed layer was in-situ annealed by raising the temperature to ~180°C. Then alternating $Ge_2Sb_2Te_5$ (GST) and Sb_2Te_3 layers were sputtered at ~180°C. Both Sb_2Te_3 and GST layers were sputtered using 30 W RF power with 30 sccm Ar at a deposition pressure of 4 mTorr. The total thickness of the superlattice was ~65 nm including the seed layer. The alternating GST and Sb_2Te_3 layer thicknesses were varied to achieve SLs with different period thicknesses (while keeping the total thickness of the SL stack same). Finally, without breaking the vacuum, a 10 nm TiN capping layer was deposited *in situ* at room temperature to protect the phase change layers from oxidation. For all the depositions, the base pressure of the sputtering chamber was maintained at $<10^{-7}$ Torr.

Section 2. Fabrication Process of Superlattice Phase Change Memory Device

We fabricated mushroom-cell SL-PCM device with Sb_2Te_3/GST superlattice (SL) phase change material on a TiN bottom electrode (BE). Prior to the deposition of the SL, the BE surface was cleaned in situ by Ar etching to remove any native oxide. Then the superlattice layers (including the 10 nm TiN capping layer) were deposited using the same deposition method and condition detailed in **Supporting Information Section 1**. Next, we patterned and etched the device region by reactive ion etching with 30 sccm Cl_2 / 5 sccm BCl_3, 10 sccm Ar, 60 W RF power at a pressure of 10 mTorr. Next, after doing an *in-situ* Ar sputter cleaning for 2 minutes to remove any native TiO_x layer, we sputtered additional 20 nm TiN followed by 60 nm Pt as the top electrode (defined by lift-off process).

Section 3. Supplementary Figures

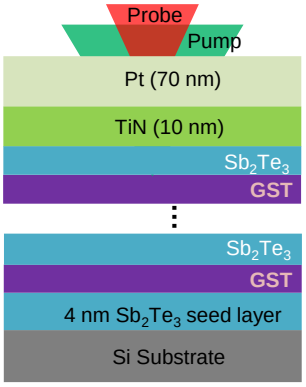

Figure S1: Schematic of the material stack used for the effective thermal conductivity measurement using time domain thermoreflectance (TDTR) showing bottom to top: silicon (Si) substrate, 4 nm Sb_2Te_3 seed layer, deposited alternating $Ge_2Sb_2Te_5$ (GST) and Sb_2Te_3 superlattice layers, 10 nm TiN capping layer and 70 nm Pt transducer layer (all sputter deposited in-situ) and pump/probe.

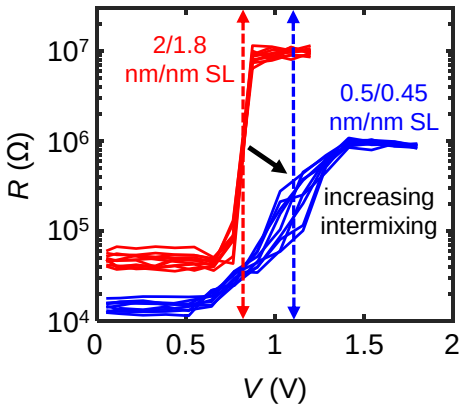

Figure S2: Resistance (*R*) vs. voltage (*V*) comparing well-cycled SL-PCM devices (~110 nm BE diameter) having different degree of intermixing within their SL interfaces. A higher switching voltage is measured in a 0.5/0.45 nm/nm SL-PCM device with stronger intermixing compared to 2/1.8 nm/nm SL-PCM device with good quality interface (also see relevant STEMs in main text Figure 1b-d). Vertical dashed lines represent switching voltage defined by the voltage (*V*) required for at least a ~10x change in *R*.

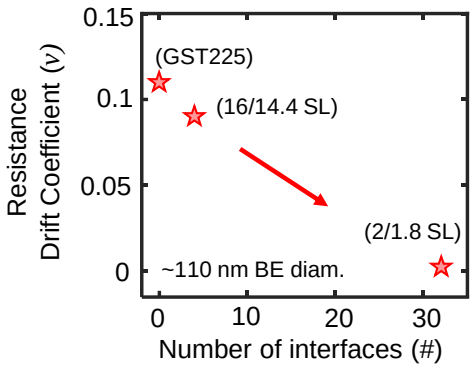

Figure S3: Resistance drift coefficient (ν) vs. number of interfaces for PCM devices (all with the same ~110 nm BE diameter). ν for the highest resistance state in 2/1.8 nm/nm SL with 32 internal interfaces decreases compared to 16/14.4 nm SL with 4 internal interfaces and GST (with no internal interface) PCM.

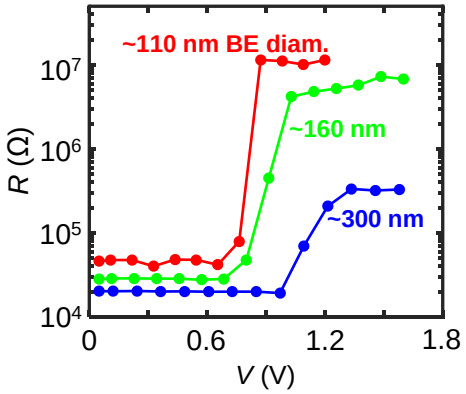

Figure S4: Resistance (R) vs. voltage (V) for 2/1.8 nm/nm SL-PCM device with different BE diameter (here from ~300 nm to ~110 nm).

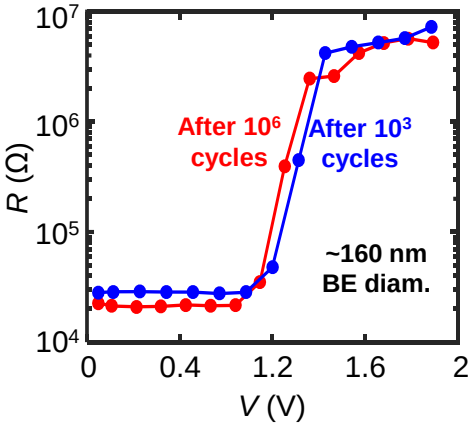

Figure S5: R vs. V after 10^3 (in blue) and 10^6 (in red) switching cycles showing that switching voltage is preserved in our Sb_2Te_3/GST 2/1.8 nm/nm SL-PCM device even after extensive electrical cycling (here shown for a device with ~160 nm BE diameter).