Ultrathin Three-Monolayer Tunneling Memory Selectors

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ABSTRACT: High-density memory arrays require selector devices, which enable selection of a specific memory cell within a memory array by suppressing leakage current through unselected cells. Such selector devices must have highly nonlinear current−voltage characteristics and excellent endurance; thus selectors based on a tunneling mechanism present advantages over those based on the physical motion of atoms or ions. Here, we use two-dimensional (2D) materials to build an ultrathin (three-monolayer-thick) tunneling-based memory selector. Using a sandwich of h-BN, MoS_2, and h-BN monolayers leads to an "H-shaped" energy barrier in the middle of the heterojunction, which nonlinearly modulates the tunneling current when the external voltage is varied. We experimentally demonstrate that tuning the MoS_2 Fermi level can improve the device nonlinearity from 10 to 25. These results provide a fundamental understanding of the tunneling process through atomically thin 2D heterojunctions and lay the foundation for developing high endurance selectors with 2D heterojunctions, potentially enabling high-density non-volatile memory systems.

KEYWORDS: 2D material, heterojunction, selector, h-BN, MoS₂, graphene, tunneling barrier
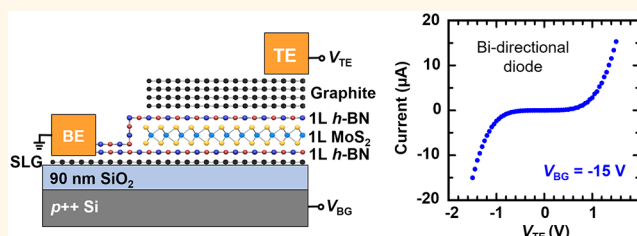
Much research has recently focused on emerging non-volatile memory technologies, such as resistive random-access memory (RRAM) and phase change memory (PCM), because of their potential for building high-density cross-point memory arrays. In this memory array architecture, the unselected word lines and bit lines are biased with half of the program voltage, potentially causing a leakage current through unselected low resistance state (LRS) cells and decreasing the read and write margin.[1] To enable such technologies, a two-terminal memory selector with highly nonlinear current−voltage $(I−V)$[2,3] behavior is needed to pair with each memory cell. The selector should be stacked vertically with the memory cell to form a 1 selector-1 resistor (1S1R) cell in a cross-point architecture.[4−6] This selector device connected in series with the memory cell will block current at low voltage (off-state) while allowing higher current at high voltages (on-state) in both positive and negative voltage polarities. The 1S1R cell enables reading and writing a memory cell at the intersection of the selected bit line and selected word line in a cross-point memory array.

The realization of chalcogenide phase-change selector technology (*i.e.*, Ovonic threshold switches or OTS) enabled commercialization of PCM storage-class memory.[7] In this 1S1R integration, the selector must be turned on for every write *and* read operation; thus its endurance must be significantly greater than the write endurance of the companion memory.[8] For memories that are heavily used during computation, such as on-chip cache or main memory, the selector endurance should exceed $\gtrsim 10^{12}$ cycles (Supporting Information Section 1). However, threshold-type selectors (such as the chalcogenide phase-change selector mentioned above) generally suffer from low endurance ($<10^6$) and cycle-to-cycle variation of threshold voltage.[9−11] On the other hand, memory selectors based on quantum tunneling can be expected to have virtually unlimited endurance, fast speed, and low cycling variation. An example of the high endurance of a tunnel barrier is the MgO tunnel barrier of spin-transfer torque magnetoresistive RAM (STT-MRAM).[12]

Previous research has shown that a heterojunction-based selector can provide sufficiently nonlinear $I−V$ with proper band gap engineering.[8,13−15] A high nonlinearity >10^4 (defined as the current at full-read voltage, V_{READ}, divided by the current at $V_{READ}/2$) was observed experimentally for a $Ta_2O_5/TaO_x/TiO_2$ tri-layer structure.[13] The nonlinearity is attributed to a
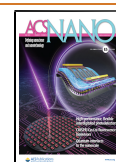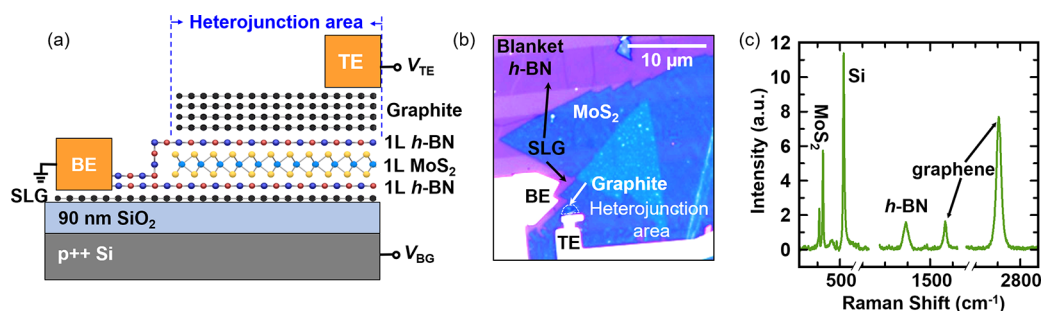
Figure 1. (a) Cross-sectional schematic of the H-shaped heterojunction (h-BN/MoS$_2$/h-BN). We use single-layer graphene (SLG) and graphite as electrodes for measuring the tunneling current through the heterojunction. (b) Optical image showing a top view of the H-shaped device. (c) Raman spectroscopy measurements on the H-shaped device after fabrication, showing clear signals of h-BN, graphene, MoS$_2$, and the Si substrate.
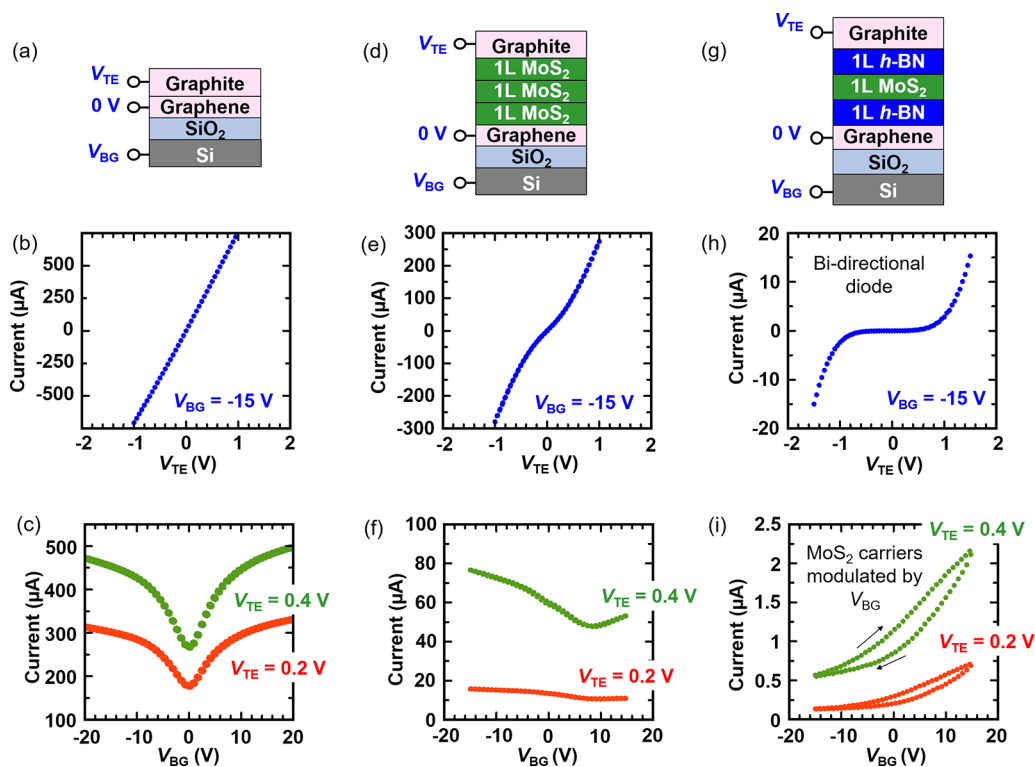

Figure 2. Tunneling current characterizations of control samples and H-shaped device. (a) Schematic of graphene-graphite measurement. (b) The tunneling current varied with V_{TE} at fixed $V_{BG} = -15$ V, showing simple resistor behavior. (c) The tunneling current varied with V_{BG} at fixed $V_{TE} = 0.2$ and 0.4 V. The tunneling current shows ambipolar behavior from modulating the work function of graphene with V_{BG}. (d) Schematic of the 3×MoS$_2$ measurement. (e) The tunneling current varied with V_{TE} at fixed $V_{BG} = -15$ V, showing an almost-linear $I-V_{TE}$, indicating no energy barrier in the junction. (f) The tunneling current varied with V_{BG} at fixed $V_{TE} = 0.2$ and 0.4 V. The tunneling current also shows an ambipolar behavior, indicating the resistance is dominating by graphene/graphite. The Dirac point is shifted away from 0 V due to doping from the fabrication process. (g) Schematic of the H-shaped measurement. (h) The tunneling current varied with V_{TE} at fixed $V_{BG} = -15$ V, showing a symmetric bidirectional diode behavior. This nonlinear $I-V_{TE}$ indicates an energy barrier in the heterojunction. (i) The tunneling current varied with V_{BG} at fixed $V_{TE} = 0.2$ and 0.4 V. The tunneling current increases with higher V_{BG}, confirming that V_{BG} is modulating the MoS$_2$ Fermi level. All measurements are performed at room temperature.

specially designed tunneling barrier in which a smaller band gap material is sandwiched between two larger band gap materials.[8,13,16] Despite the quantum tunneling mechanism, oxide traps and surface dangling bonds in such materials still limit the endurance and the current drive. In this respect, ultrathin two-dimensional (2D) materials are more promising for a heterojunction tunnel barrier, because they offer a wide range of choices for band gap engineering,[17] and they do not suffer from surface dangling bonds. Recent simulations of tunnel barriers using 2D materials with metal electrodes

suggest that the tri-layer structure with a smaller band gap 2D semiconductor sandwiched by a large band gap h-BN ($E_G \approx 6$ eV)[18] can lead to high on-current due to the small tunneling distance, while maintaining high nonlinearity (more discussion in Supporting Information Section 2).[19] As the energy band diagram of this structure resembles the letter "H", this tri-layer structure is referred to as an "H-shaped" heterojunction.

In this work, we utilize the 2D materials h-BN and MoS$_2$ to demonstrate an ultrathin (three-monolayer-thick) tunneling-based memory selector. The fabrication process for the H-
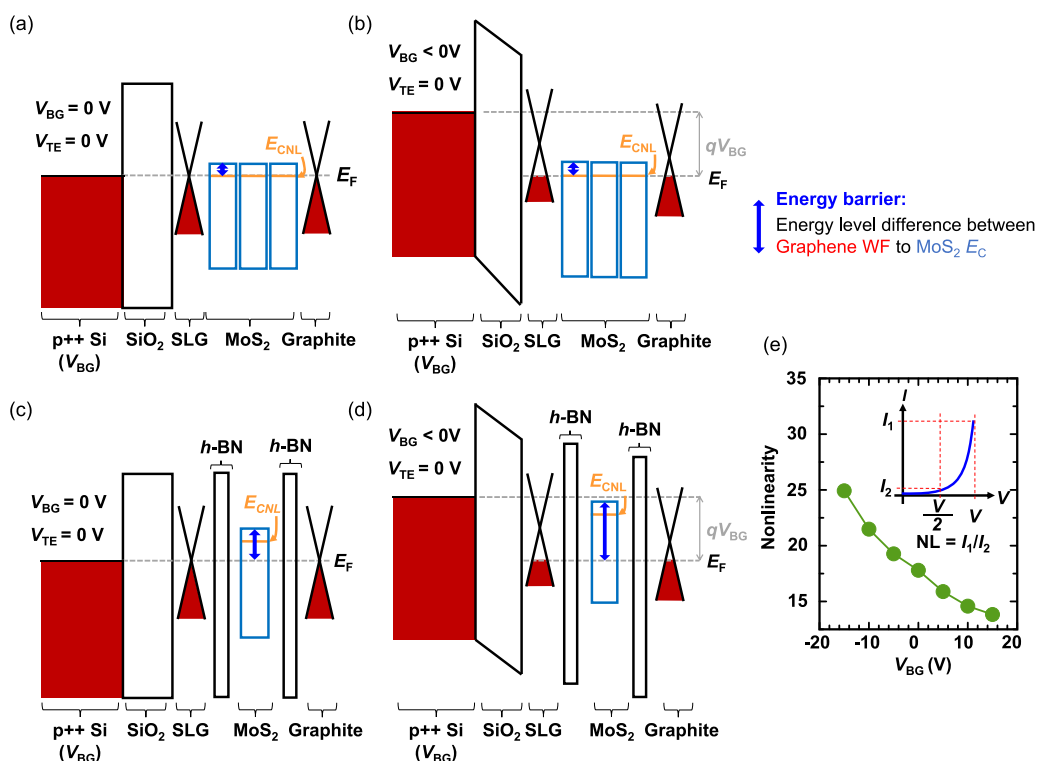
Figure 3. Comparison of the 3×MoS₂ and H-shaped structures. (a) The energy band diagram of 3×MoS₂ at V_{BG} = 0 V and V_{TE} = 0 V. The work function (WF) of graphene/graphite and the Fermi level of MoS₂ are pinned to E_{CNL} of MoS₂. (b) The energy band diagram of 3×MoS₂ at V_{BG} < 0 V and V_{TE} = 0 V. As the Fermi level of MoS₂ is pinned to its E_{CNL}, the energy barrier does not change with V_{BG}. (c) The energy band diagram of the H-shaped heterostructure at V_{BG} = 0 V and V_{TE} = 0 V. The h-BN between MoS₂ and graphene/graphite electrodes de-pins the MoS₂ Fermi level from its E_{CNL}. (d) The energy band diagram of the H-shaped heterostructure at V_{BG} < 0 V and V_{TE} = 0 V. The energy barrier increases as V_{BG} electrically lowers the electron carrier concentration in the MoS₂. (e) The nonlinearity (NL) of the H-shaped device increases with lower V_{BG}. The inset figure illustrates that the nonlinearity is defined as the current at full-read voltage (V_{READ}) divided by the current at V_{READ}/2.

shaped structure meets key CMOS processing requirements by using layer transfers[20,21] to reduce the process temperature and using chemical vapor deposition (CVD) growth[20,22,23] of 2D materials to increase yield. To probe the electrical characteristics of the heterojunction, we use CVD-grown graphene as the bottom electrode (BE) and exfoliated graphite as the top electrode (TE),[24,25] avoiding potential damage or reactions with evaporated metals[26] (see Supporting Information Section 3 for more details). We conclude this report by benchmarking the H-shaped device with previous studies on 2D material vertical transport for memory selectors and review future challenges toward commercial applications.

RESULTS AND DISCUSSION

Device Design. The complete H-shaped device with CVD-grown monolayer MoS₂ sandwiched by CVD-grown monolayer h-BN[27] and graphene/graphite as the BE/TE, respectively, is shown in Figure 1a. We were able to characterize the effect of the tunnel barrier on the out-of-plane current transport by controlling the band alignment with a back-gate, whose electric field penetrates through the graphene BE, modulating the heterostructure band alignment. In this study, we first focus on understanding the underlying physics of this ultrathin tunneling heterojunction with our proof-of-concept device.

To build the H-shaped device, we transfer monolayer h-BN ($t ≈ 0.3$ nm), MoS₂ ($t ≈ 0.6$ nm), and h-BN in this order after first transferring and patterning graphene on SiO₂ as the BE.

Exfoliated graphite is then aligned and transferred as the TE to avoid overlap of the TE and BE, by choosing graphite flakes with the desired TE shape. The resulting heterojunction area is defined by the overlap of the graphene and the graphite (Figure 1b). More details of the fabrication and the transfer processes are described in the Materials and Methods section and Supporting Information Section 4. Figure 1b shows the top view optical image of a device, and Figure 1c shows the Raman spectra taken after fabrication, revealing clean MoS₂, graphene, and h-BN signals.

Electrical Characterization. The H-shaped device structure from bottom to top is graphene/h-BN/MoS₂/h-BN/graphite, with multiple interfaces that need to be characterized to understand their band alignments. Thus, we also designed two control devices: graphene/graphite and graphene/3×MoS₂/graphite, with "3×" indicating three layers of monolayer CVD MoS₂ transferred sequentially. Schematics of the two control devices and the H-shaped selector device are shown in Figure 2a,d,g. Top view optical images of the two control devices are shown in Supporting Information Section 5. We characterized the three devices by measuring their tunneling current, sweeping V_{TE} at a fixed V_{BG}. Because out-of-plane electric fields can penetrate the graphene,[25] we also characterize their tunneling current by sweeping V_{BG} at a fixed V_{TE}. For the graphene/graphite device, the tunneling current *versus* V_{TE} is linear, indicating a simple resistor (Figure 2b). In Figure 2c, sweeping V_{BG} reveals only the ambipolar behavior caused by tuning the graphene work function.
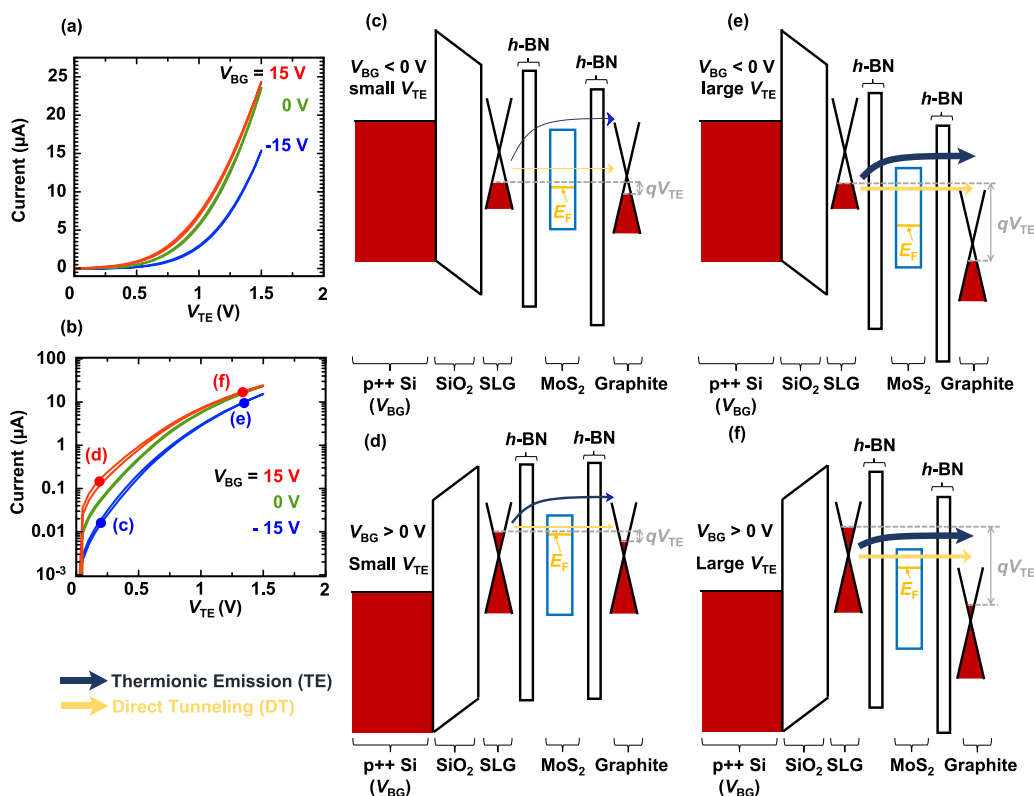
Figure 4. Measurements of tunneling current through the H-shaped device at $V_{BG} = -15$, 0, and 15 V in (a) linear and (b) log scales. (c–f) The energy band diagrams of the H-shaped device at different V_{BG} and V_{TE} biases. (c) At $V_{BG} < 0$ V and small V_{TE}, the negative V_{BG} depletes electrons in the MoS$_2$ layer; thus the current is limited by direct tunneling through 3 layers (two h-BN and one MoS$_2$ layer). (d) At $V_{BG} > 0$ V and small V_{TE}, the positive V_{BG} accumulates electrons in the MoS$_2$ layer, increasing direct tunneling and thermionic emission. (e) At $V_{BG} < 0$ V and large V_{TE}, and (f) at $V_{BG} > 0$ V and large V_{TE}, the large V_{TE} effectively lowers the MoS$_2$ energy barrier at any V_{BG}; thus most carriers pass through the MoS$_2$ layer without direct tunneling through the MoS$_2$ energy barrier. Thicker TE/DT arrows illustrate more current flowing.

We then characterized the device with 3×MoS$_2$ between graphene and graphite. Figure 2e shows that the measured $I-V_{TE}$ has weak nonlinearity, suggesting that the MoS$_2$ homojunction alone is not effective in creating a sufficiently large barrier to suppress tunneling current at low V_{TE}, and that heterojunction band gap engineering is needed to achieve higher nonlinearity. As shown in Figure 2f, the $I-V_{BG}$ data also display ambipolar behavior, indicating the resistance is dominated by the graphene/graphite. We note that the stacking angle of the MoS$_2$ could affect the valence band structure of the 3×MoS$_2$ homojunction, as suggested by previous theoretical calculations.[28] However, the electrical measurements in this work may be unaffected by this, because the conduction bands serve as the tunneling barrier.

With the H-shaped heterojunction design, we observe significantly higher nonlinearity of $I-V_{TE}$ (Figure 2h) than with the 3×MoS$_2$. The $I-V_{TE}$ of the H-shaped device presents a symmetric bipolar diode behavior desired for a memory selector. The significant current suppression at low V_{TE} indicates the existence of a higher tunnel barrier at the h-BN/MoS$_2$/h-BN junction than at high V_{TE}. Instead of the ambipolar $I-V_{BG}$ behavior observed with the graphene/graphite and graphene/3×MoS$_2$/graphite devices, the H-shaped device displays n-type semiconductor behavior due to modulation of the MoS$_2$ conductance by V_{BG} (Figure 2i). The ability to control the MoS$_2$ Fermi level confirms the existence of a tunnel barrier that can be tuned by the V_{BG}. However, we note that the $I-V_{BG}$ data has more hysteresis than the $I-V_{TE}$

data as mid-gap traps between SiO$_2$ and BE graphene are activated when sweeping V_{BG}.[29]

To illustrate the tunnel barrier of the H-shaped heterojunction, in Figure 3a–d, we compare the energy band diagram of the 3×MoS$_2$ device to the H-shaped device. Because of the atomically sharp interfaces and ultrathin 2D material layers, the energy level of each 2D material layer in Figure 3a–d will have a uniform carrier density, whereas, in conventional bulk heterojunctions, both depletion and intrinsic regions exist in the semiconductor layer at Schottky contact interfaces. The weak nonlinearity of the 3×MoS$_2$ device $I-V_{TE}$ characteristic indicates that the Fermi level of MoS$_2$ is pinned close to the conduction band, resulting in a small Schottky barrier, which has been observed before in graphene/MoS$_2$ junctions.[25] This is similarly observed in metal contacts to MoS$_2$ transistors which typically display n-type characteristics.[23] Although 2D material interfaces lack mid-gap states from dangling covalent bonds as in silicon/metal interfaces, the presence of the surface states in 2D materials often still results in strong Fermi level pinning.[30,31] These surface states could not only originate from the fabrication process but also form interface dipoles or gap states produced by interface interactions between graphene and MoS$_2$.[32] In the 3×MoS$_2$ device, the Fermi levels of graphene/graphite are pinned to the charge neutrality level (E_{CNL}) of MoS$_2$. From previous research, E_{CNL} is less than 0.2 eV below the MoS$_2$ conduction band (E_C),[33] resulting in a very small energy barrier in the heterojunction. As shown in Figure
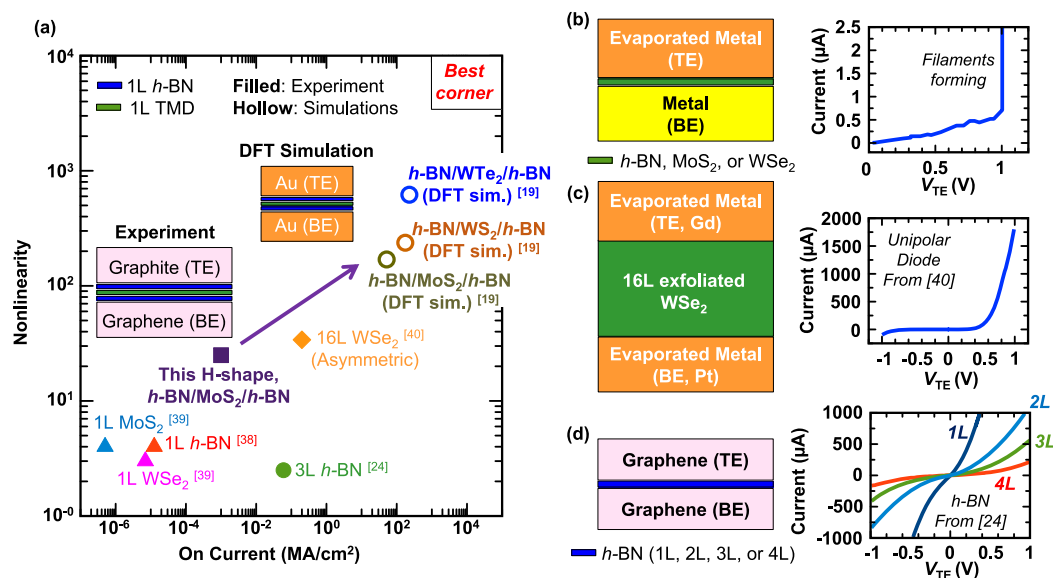
Figure 5. (a) Memory selector performance (nonlinearity *vs* on-current) benchmarking of the H-shaped device with previous simulation projections and other representative vertical transport studies on 2D materials.[19,24,38−40] (b) MIM test structures in this work (Supporting Information Section 2) with transferred CVD-grown 2D materials (MoS$_2$, WSe$_2$, *h*-BN) on metal BE and then deposited metal TE. The low current and noisy I−V$_{TE}$ indicates high contact resistance possibly between BE and transferred 2D materials. (c) The MIM structure in Nazir *et al.*[40] with a transferred 16L WSe$_2$ flake on a through-substrate hole, allowing direct metal evaporation on both sides of the WSe$_2$. The low contact resistance enables tunneling current characterization of 2D materials, but the device exhibits an asymmetric I−V$_{TE}$ as the barrier is created by an asymmetric Schottky contact. (d) Out-of-plane tunneling current through monolayer to 4L exfoliated *h*-BN with graphite as TE and BE in Britnell *et al.*[24]

3a, this low energy barrier explains the almost-linear I−V$_{TE}$ through 3×MoS$_2$.

When V$_{BG}$ is swept from zero (Figure 3a) to negative voltage (Figure 3b), the graphene/graphite work function will remain at the MoS$_2$ charge neutrality level, resulting in a fixed energy barrier independent of V$_{BG}$. On the other hand, in the H-shaped device, the MoS$_2$ and graphene/graphite electrodes are separated by monolayer *h*-BN. The *h*-BN is an interfacial layer which limits the impact from surface dipoles and de-pins the MoS$_2$ Fermi level from its E$_{CNL}$ (Figure 3c).[20] Thus, the MoS$_2$ energy barrier seen by electrons at V$_{BG}$ = 0 V is the energy level difference of the graphene work function and the MoS$_2$ E$_C$ (Figure 3c). The Fermi level of MoS$_2$ can be modulated by V$_{BG}$, leading to an increased energy barrier with V$_{BG}$ < 0 V (Figure 3d). As discussed in Supporting Information Section 6, the de-pinning effect of the *h*-BN layer is also observed in asymmetric heterojunctions (graphene/*h*-BN/MoS$_2$/graphite and graphene/MoS$_2$/*h*-BN/graphite).

The modulation of the tunnel barrier is essential to sufficiently suppress the off-state current. Figure 3e summarizes how modulating the energy barrier increases the memory selector nonlinearity from 10 to 25. Figure 4a,b shows that, by decreasing V$_{BG}$ from 15 to −15 V, the off-current decreases by 10× but the on-current only decreases by 40%. The nonlinearity of the 2D selector is modulated by V$_{BG}$, and this nonlinearity is clearly a result of the energy barrier in the heterojunction, not surface contamination due to the transfer process. This electric field modulation mechanism provides the key insight into how changing the band alignment and Fermi level of the middle semiconductor layer can improve tunneling-based selector I−V nonlinearity for designing a two-terminal selector.

Figure 4c−f uses energy band diagrams to illustrate the charge transport mechanisms through the vertical H-shaped

heterojunctions at different V$_{BG}$ and V$_{TE}$ biases. As the electron affinity of *h*-BN (χ ≈ 2.3 eV)[34] is much smaller than the work function of graphene/graphite (∼4.6 eV),[35,36] thermionic emission over the *h*-BN barrier is negligible at all V$_{BG}$ and V$_{TE}$ biases. Therefore, the MoS$_2$ energy barrier height is essential for suppressing the off-state current and increasing the I−V$_{TE}$ nonlinearity. For the off-state current, the H-shaped device is measured at small V$_{TE}$ (Figure 4c,d). As illustrated in Figure 4c, negative V$_{BG}$ increases the MoS$_2$ energy barrier, limiting off-state current by decreasing direct tunneling through three monolayer 2D materials (*h*-BN/MoS$_2$/*h*-BN). Conversely, positive V$_{BG}$ lowers the MoS$_2$ tunnel barrier, increasing the direct tunneling transmission and thermionic emission through the MoS$_2$, causing a higher off-state current (Figure 4d). For on-current, the H-shaped device is biased at large V$_{TE}$ which effectively lowers the MoS$_2$ energy barrier at both negative V$_{BG}$ (Figure 4e) and positive V$_{BG}$ (Figure 4f). As most carriers can pass through the MoS$_2$ layer without direct tunneling through the MoS$_2$ energy barrier at large V$_{TE}$, the on-currents are similar at any V$_{BG}$. Comparing the H-shaped to the 3×MoS$_2$ device, the on-current of the H-shaped device (Figure 2h, 16 μA, heterojunction area: 1.6 μm^2) is lower than that of the 3×MoS$_2$ device (Figure 2e, 300 μA, homojunction area: 15 μm^2). This is partly because the on-current through 3×MoS$_2$ is only limited by the van der Waals gaps due to the negligible MoS$_2$ energy barrier, while the on-current through the H-shaped heterojunction is limited by the wide band gap *h*-BN layers.

While the ultrathin H-shaped heterojunction should have high current, high endurance, and sufficient nonlinear I−V$_{TE}$, the experimental results presented here do not surpass the performance of threshold-type selectors based on atomic motion.[11] In Supporting Information Section 7, we note that the lateral parasitic resistances are negligible in the H-shaped

device; therefore, we can derive the current density by assuming that the effective heterojunction area is the overlap of the BE graphene and the TE graphite. From this analysis, the H-shaped device has a current density of 1 kA/cm² (= 16 μA/1.6 μm²) at V_{TE} = 1.5 V, nonlinearity of 25 at V_{TE} = −1.4 V, and the off-current increases after 100 cycles. This limited performance is most likely due to interlayer contamination and traps resulting from the multiple transfer process steps.

Benchmarking. Interestingly, earlier simulations have suggested that a selector nonlinearity over 100 could be adequate for terabit memory arrays, such as 3D vertical RRAM.[1] Since the nonlinearity of our experimental H-shaped device is only 4× away from this goal, we are optimistic that H-shaped devices can reach the required performance by improving their on-current density. In Figure 5, we compare the H-shaped device performance to the previous simulations of H-shaped devices with Au electrodes and using WTe₂, MoS₂, and WS₂ monolayers as the middle 2D semiconducting material.[19] The results indicate a pristine 2D material H-shaped device could reach current densities of 20 MA/cm² which is higher than the chalcogenide phase-change selector record high current density of 2 MA/cm².[37]

Figure 5 also presents other representative 2D experimental studies. In a metal-insulator-metal (MIM) structure fabricated by transferring 2D monolayers (h-BN, WSe₂, and MoS₂) onto a metal BE, the tunneling current should be very high due to the small tunneling distance, but the experimental results show a very low and noisy current, eventually breaking down at high voltage as shown in Figure 5b (more discussion in Supporting Information Section 3).[38,39] In a separate study,[40] a MIM structure fabricated by transferring exfoliated 16-layer WSe₂ on a through-substrate hole, then evaporating both BE and TE on WSe₂ directly, resulted in a much lower contact resistance. As such, the $I–V_{TE}$ of this device shows higher current density and a smoother diode behavior.[40] However, this tunnel barrier is created by an asymmetric Schottky contact resulting in asymmetric $I–V_{TE}$, thus limiting the use of such device structures as a memory selector, which typically require symmetric $I–V_{TE}$. Lastly, the study of direct tunneling through h-BN characterized in a structure with transferred graphene as TE and BE[24] shows similar low nonlinearity as our 3×MoS₂ homojunction device, confirming that devices without heterojunctions are insufficient for selector applications. The limitations of these previous device designs highlight the benefits of H-shaped heterojunctions.

To improve the H-shaped device performance toward the simulation projections, future work must focus on improving the metal-2D interface to increase on-current and nonlinearity. Such solutions could be achieved by using atomic layer deposition of metals to eliminate damage from metal evaporation and reduce surface roughness, and adopting a dry 2D material transfer process or direct low-temperature growth to reduce contamination at the 2D material interfaces. It is also important to mention that the nonlinearity can be improved by optimizing the energy band gap and thickness of the H-shaped device.[19] Additionally, we calculated the current density of our H-shaped device using the entire heterojunction cross-sectional area, which is likely an underestimation because current will not flow evenly throughout the junction area. Future work should focus on area-scaling of the H-shape to calculate the true current density.

CONCLUSIONS

We have demonstrated out-of-plane tunneling current through a 2D material H-shaped heterojunction, a promising memory selector candidate. In the H-shaped device design, the nonlinearity of the 2D heterojunction can be controlled by shifting the MoS₂ Fermi level with a back-gate voltage. These electrically tunable characteristics suggest that the nonlinearity can be improved by using chemical or charge transfer doping of the middle semiconductor layer. The nonlinearity of our selectors must be improved by at least a factor of 4× in order to be adequate for terabit memory arrays. This could be achieved with optimized band gap engineering, improved material quality and metal-2D interfaces, and cleaner direct growth or transfer techniques. This work reveals useful insights in ultrathin heterojunctions and introduces a promising candidate for memory selector applications.

MATERIALS AND METHODS

H-Shaped Device Fabrication. Figure 1 is the cross-sectional schematic of the H-shaped device, a stack of graphene/h-BN/MoS₂/h-BN/graphite heterojunction fabricated on a 90 nm SiO₂/p⁺⁺ Si substrate (0.001−0.005 Ω·cm) by transferring the 2D materials layer by layer in air.[21] All monolayer materials are grown by large-area chemical vapor deposition (CVD),[23,27] except the top-electrode (TE) graphite flakes are exfoliated from bulk crystals. We used MoS₂ as the middle material in the H-shaped heterojunction due to its availability as high quality grown films in our laboratories.[23] Monolayer MoS₂ is grown on a 90 nm SiO₂/Si substrate in single crystalline and continuous polycrystalline regions using a solid-source CVD process.[41] Continuous, centimeter-scale h-BN monolayer was grown on a reusable Pt foil via low-pressure CVD at 1100 °C.[20] Monolayer graphene is first grown on a Cu foil by CVD at 1060 °C, using CH₄ carbon source.[42] We then transfer the graphene onto SiO₂ and pattern it into stripes with e-beam lithography, followed by oxygen plasma to selectively etch the graphene. Detailed transfer techniques for each material are further elaborated in Supporting Information Section 4. After forming the heterojunctions graphene/h-BN/MoS₂/h-BN, we transfer exfoliated graphite flakes on top as the TE. The last step is to pattern the Pd metal leads on BE (monolayer graphene) and TE (graphite flake) and electrical pads for the electrical characterization.

Electrical and Raman Characterization. All electrical measurements were taken in a probe station in a vacuum of ~5 × 10⁻⁵ Torr in the dark, at room temperature. All electrical measurements plotted include both forward and backward sweeps. Figure S6.1 plots the current from all three terminals (I_{TE}, I_{BE}, I_{BG}), showing that the gate leakage (I_{BG}) current is much lower than I_{TE} and I_{BE}, which have nearly identical magnitude. We note the depletion capacitance of the p⁺⁺ silicon back-gate will reach a minimum of ~760 nF/cm² at a V_{BG} = −15 V, decreasing the gate capacitance from ~38 to ~37 nF/cm² and therefore having little impact on the $I–V$ data measured in this study. All Raman characterization used a 532 nm laser and 1800 g/mm.

ASSOCIATED CONTENT

ⓢ Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.1c00002.

Memory selector endurance requirement; DFT simulation of the H-shaped devices; MIM structure with metal electrodes; fabrication and transfer process of the H-shaped device; optical images of devices measured in Figure 2; asymmetric heterojunction; lateral parasitic resistances of the H-shaped devices (PDF)

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Notes

The authors declare no competing financial interest.

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Supporting Information for:

Ultrathin Three-Monolayer Tunneling Memory Selectors

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1. Memory Selector Endurance Requirement

One of the motivations of using tunnel barrier is its virtually unlimited endurance by utilizing the quantum tunneling mechanism. Modern commercial products utilize a 1 selector-1 resistor (1S1R) architecture with chalcogenide phase-change selector that have endurances typically less than 10^6 cycles. The limited endurance is inevitable as threshold-type selector technologies are sensitive to local Joule heating, including selectors based on chalcogenide phase-change,[1,2,3] oxide phase-change (such as NbO_2),[4-6] and volatile ion motion.[7-9] In an efficient computer architecture, in order to reduce latency and cost, the central processing unit (CPU) accesses data based on a computer memory hierarchy (Fig. S1), where memories closer to the CPU are accessed more often and must be fast in response time but have high cost per byte, whereas memories further away from the CPU are cheaper but slower in response time and accessed less often. As a result, the memories closer to the CPU require higher endurance as they are accessed more frequently. Commercial 1S1R crossbar products currently serve as storage class memory, lying between memory and storage in memory hierarchy, due to its limited endurance. To push the 1S1R applications towards main memory or cache, the endurance must be higher than storage-class memory.

In order to estimate the required endurance of the 1S1R structure for applications that require frequent access, we calculate the number of cycles for a 10-year lifetime with assumed cycle time and access frequency. As according to the previous study,[10] the write latency of the commercial product is 94 ns, here we assume the memory cycle time is 100 ns. The worst case is writing a same cell for 10 years and the selector must achieve 3.15×10^{15} cycles. Fortunately, we can easily avoid this worst case by proper architectural design. If we assume the memory architecture contains 10^3~10^4 word lines (WL) and each WL is accessed

uniformly, the selector will be turned on about 10^{11}~10^{12} times (on average, assuming proper wear-leveling protocols are employed), which should be achievable with our H-shape selector.
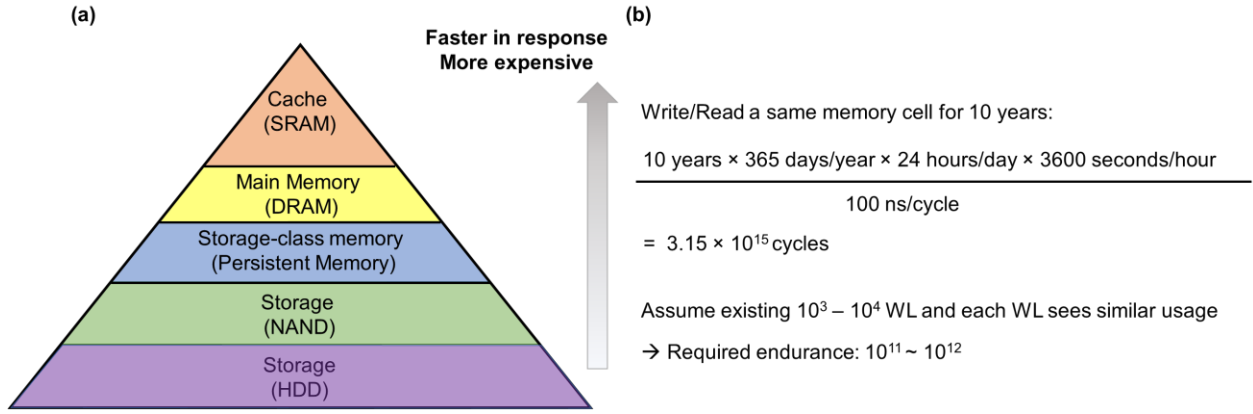

Fig. S1. (a) The memory hierarchy in a computing system. Total memory capacity of a computer can be visualized by hierarchy of components. Computer storage in low hierarchy has larger storage than that in high hierarchy as it is cheaper in cost. (b) The required endurance for memory to have a 10-year life time.

2. DFT simulation of the H-shape Devices

Density function theory (DFT) simulations[11] can provide insight into 2D heterojunctions considering quantum mechanical effects. In Fig. S2, we simulate multiple heterojunctions with Au electrodes, eliminating all parasitic resistances (graphene/graphite series resistances, contact resistance, *etc.*). In Fig. S2a,b, the I-V_{TE} of monolayer h-BN and monolayer MoS_2 simulation shows very linear behavior. The nonlinearity is slightly increased with the h-BN-MoS_2 heterojunction design (Fig. S2c). The H-shape shows nonlinearity ~100 with the h-BN-MoS_2-h-BN H-shape structure (Fig. S2d). We note that the simulation here does not consider the Fermi-level tuning of MoS_2 as observed in our experiments. As discussed in the main text, the off-current could be suppressed by tuning the MoS_2 Fermi-level to make the MoS_2 more intrinsic.

3. MIM Structure with Metal Electrodes

Reducing contact resistances of both the top electrode (TE) and bottom electrode (BE) is key for characterizing the out-of-plane tunneling current of a heterojunction. Although many studies of metal contacts on 2D materials have shown contact resistance lower than 1 kΩ·μm,[12,13] there are challenges of using metal electrodes in a metal-insulator-metal (MIM) structure for 2D material tunneling current characterization. To illustrate these issues, we summarize the electrical characterization of our previous MIM structures using Au TE and BE, with either MoS_2 or h-BN as the middle dielectric layer. To build this MIM structure (Fig. S3a-c), we pattern and deposit metal as the BE using electron beam (e-beam) lithography with A5
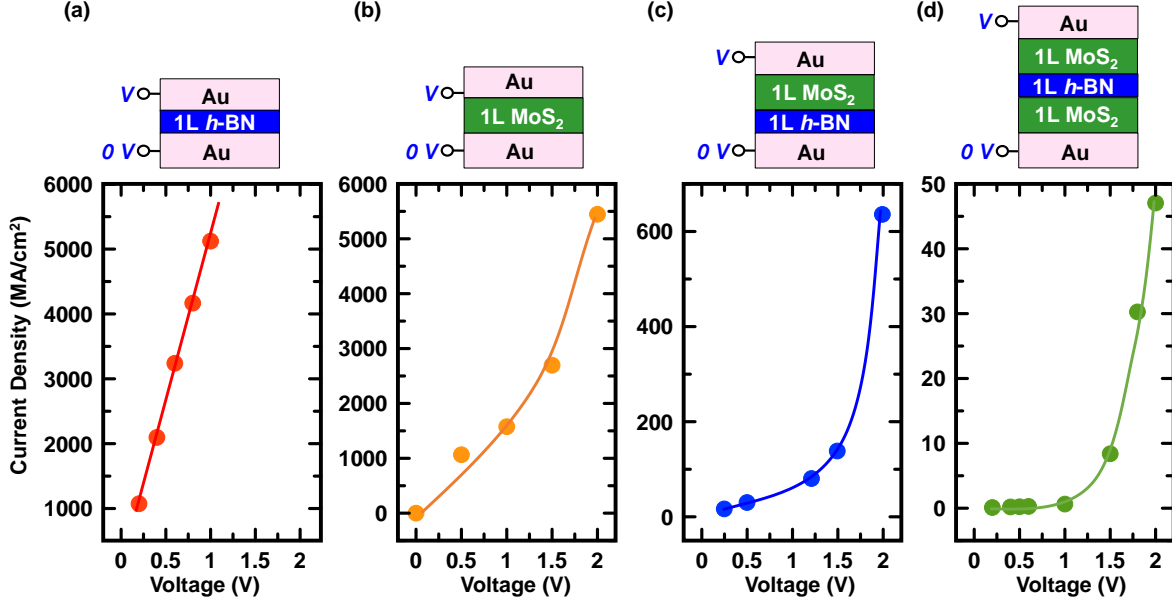
Fig. S2. DFT simulation of: (a) monolayer *h*-BN, (b) monolayer MoS₂, (c) *h*-BN-MoS₂, (d) *h*-BN-MoS₂-*h*-BN. The dots are single simulation points and line is drawn to guide the eye. We note the tunneling current densities calculated here can be high, but comparable to those observed in similar materials like carbon nanotubes, graphene, and cross-plane single layer *h*-BN.[9,14,15] In practice, scattering (in the metal electrodes and the "sandwiched" material) is expected to partly reduce the maximum current densities.

PMMA liftoff and e-beam evaporation, followed by transferring 1L *h*-BN or 1L MoS₂. Next, we pattern and deposit e-beam evaporated Al_2O_3 (~65 nm) at low pressure ($<10^{-6}$ Torr) to electrically isolate the TE and BE, and then complete the device by patterning and depositing the TE metal using e-beam evaporation at 8 kV acceleration voltages. We used electrical measurements to confirm the insulating behavior of Al_2O_3. We fabricated three different MIM devices as shown in Fig. S3a-c and summarize their electrical characterization in Fig. S3d.

Figure S3a shows a device schematic with metal on 1L MoS₂ as the TE. The I-V_{TE} of this device shows very low current (Fig. S3d). As the 1L MoS₂ is only 0.615 nm thick,[16] tunneling current through the MoS₂ should be quite high, and this low current indicates a high external contact resistance preventing any characterization of tunneling through the MoS₂. The high contact resistance is likely not from the TE contact, as many studies have characterized e-beam evaporated Au on MoS₂ with contact resistance ranging between 480 $\Omega \cdot \mu m$ to 5 $k\Omega \cdot \mu m$ resistance,[12,13,17,18] which is < 5% resistance of our MIM devices. Thus, the high contact resistance is likely from the BE, as this contact was formed by transferring CVD MoS₂ on the metal electrode, which can have surface roughness or surface contamination and impurities from the 2D material transfer process. This high contact resistance between BE and 2D material is the main motivation for using a graphene as the BE. Atomic Force Microscope (AFM) measurement on Au surface immediately after deposition shows that the surface roughness root-mean-square rms ≈ 0.58 nm (In Fig. S3e). We attempted

a vacuum anneal at 450 ℃ in order to flatten the metal surface with metal reflow (In Fig. S3f). However, the surface roughness becomes worse (rms ≈ 1.2 nm) after the anneal, possibly due to segregation around surface impurities.

In Fig. S3b, we characterized 1L h-BN with the same MIM design. Contrary to the low current in metal-MoS$_2$-metal, the h-BN device displays high current and linear I-V_{TE}, suggesting the TE and BE are shorted. This electrical shortage is observed among more than 20 devices with area less than 1 μm^2. As h-BN is only a 0.3 nm single atomic layer and easier to tear during the transfer process, the surface damage caused by e-beam evaporation is more likely to cause an immediate electrode shortage than the thicker MoS$_2$ structure.[19] The metal deposition damage likely occurred due to high-energy metal particles. In Fig. S3c, instead of using metal evaporation, we transferred metal as the TE to avoid damaging the 2D material surface. The I-V_{TE} characteristics show no short between TE and BE, even with only a single h-BN insulating layer. However, the device with transferred TE also exhibits high contact resistance between BE and 2D material, as discussed previously. As shown in the main text, we used a graphene BE to achieve an ultra-smooth contact with the H-shape device. In order to maintain a symmetric device structure, we used transferred graphite as TE, thereby also avoiding electrical shortage and possible surface damage from the e-beam evaporation.
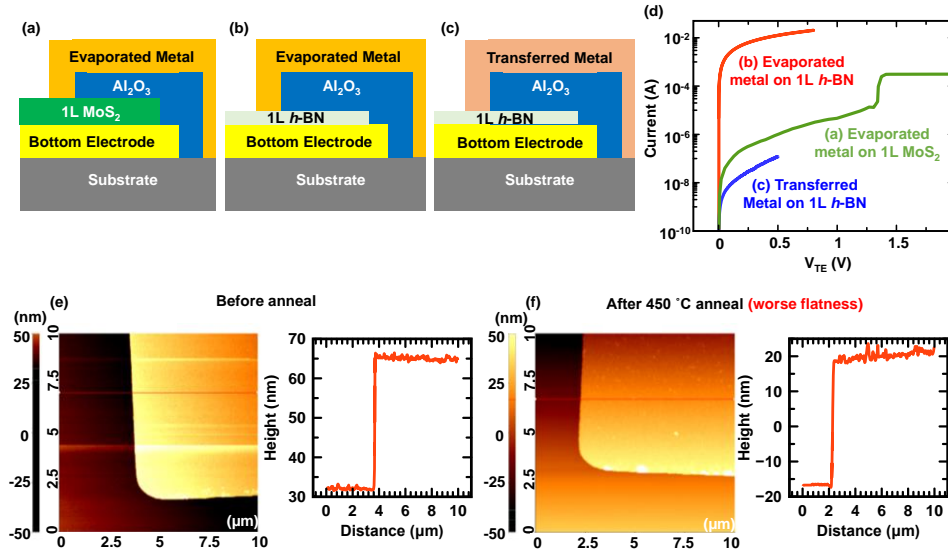

Fig. S3. The schematics of the MIM design for (a) Au-h-BN-transferred Au (b) Au-h-BN-evaporated Au (c) Au-MoS$_2$-Au (d) The I-V_{TE} characteristic of the different MIM designs. (e) AFM measurement on Au surface immediately after deposition, and (f) after vacuum anneal at 450 ℃.

4. Fabrication and Transfer Process of the H-shape

In order to build our ultra-thin heterojunction, we designed a fabrication flow integrating several 2D material transfer techniques. The fabrication steps are illustrated in Fig. S4. The details of transfer techniques

for each material are introduced separately in sections 4.1, 4.2, 4.3, and 4.4. We use e-beam lithography instead of photolithography for all the patterning steps to avoid photoresist, which introduces more contaminants than e-beam resists. We first transfer CVD continuous graphene onto a SiO_2 on p^{++} Si substrate (Fig. S4, Step 1, details in section 4.2) and then use e-beam lithography and O_2 plasma etching to pattern graphene into stripes (as shown in Fig. S4ab, Step 2) which serve as the BE layer of the heterojunction. After the BE layer fabrication, we then transfer h-BN and/or MoS_2 on top of the graphene stripes. For example, for an H-shape device, we transfer CVD 1L h-BN (Fig. S4, Step 3), CVD 1L MoS_2 (Fig. S4, Step 4), and CVD 1L h-BN (Fig. S4, Step 5) sequentially.

The transfer techniques for MoS_2 and h-BN are discussed in sections 4.1 and 4.3, respectively. Our CVD growth process of MoS_2 can produce continuous monolayer film at the center of the substrate and isolated single-grain triangles at the edge.[20] We only use the edge of the substrate because selectively transferring single MoS_2 triangles (as shown in Fig. S4ab, Step 4) is essential to our device design. The TE exfoliated graphite is then transferred on top of the graphene-h-BN-MoS_2-h-BN stack using a rotationally aligned dry transfer technique.[21] By using exfoliated graphite, we can avoid the overlap of the TE and BE by choosing graphite flakes with the desired TE shape and align transferring. The H-shape stack is finished and the resulting heterojunction area is defined by the overlap of the graphene and the graphite (Fig. S4a, Step 6). We note that it is necessary to examine every CVD film under a microscope to confirm no visible tears/wrinkles are near the heterojunction area, as these would result in a poor interface quality

After the stack of graphene (BE)-h-BN-MoS_2-h-BN-graphite-(TE) is formed, we fabricate electrical pads for probing (In Step 7&8 of Fig. S4). Since we need to avoid leakage current paths through graphene underneath the electrical pads of BE and TE, we use O_2 plasma to etch away graphene and other 2D material layers after pattern development (Step 7 of Fig. S4) and then deposit SiO_2 (20 nm)/Ti (5 nm)/Au (40 nm) for the 150×150 μm electrical pads (Step 8 of Fig. S4) using e-beam evaporation at low pressure ($<10^{-6}$ Torr). Though e-beam evaporated SiO_2 layer has lower breakdown voltages than thermal SiO_2 on Si, SiO_2 under the Ti/Au pads provides enough extra isolation between the pads and global back-gate to reduce gate leakage current. As such, it is necessary to deposit the probing pads before fabricating contacts to the graphene and graphite electrodes.

Next, we fabricate Pd leads to connect BE and TE to electrical pads (Fig. S4, Step 9).[22] It is essential to selectively transfer isolated single-grained MoS_2 triangles as shown in Step 4 of Fig. S4, so Pd leads can form direct contact with graphene BE that is not covered by MoS_2. However, the BEs are still underneath 2 layers of h-BN as we transferred two ~5×5 mm continuous h-BN film in the H-shape fabrication. As observed from the experimental result in Fig. S4b, evaporated metal on top of 1L h-BN will certainly short

with BE even with less than 1 µm² contact area on *h*-BN without visible tears. The contact area of Pd leads on graphene BE is usually > 10 µm² and appears to still be in contact with graphene in our fabrication. As *h*-BN is an electrically isolating layer due to its large bandgap, depositing Pd leads directly on *h*-BN does not create a lateral leakage path. The H-shape device is then finished and ready for electrical measurements.

The Pd leads on graphene BEs should not overlap with the semiconducting MoS$_2$ layer (Step 7 of Fig. S4) as this overlap would create a possible leakage current path through MoS$_2$, resulting in a higher off-current. This current is not obvious as the MoS$_2$ sheet resistance is much lower than the graphene sheet resistance, especially when the carrier density of MoS$_2$ is decreased at negative back-gate voltage. As such, in devices of Fig. S4ab, the metal contacts to graphene (BE) are slightly in contact with the MoS$_2$ layer but the devices still exhibit nonlinear diode behavior. However, we try to avoid this overlap of the Pd leads and MoS$_2$ layer as this leakage current degrades the nonlinearity of the selector.
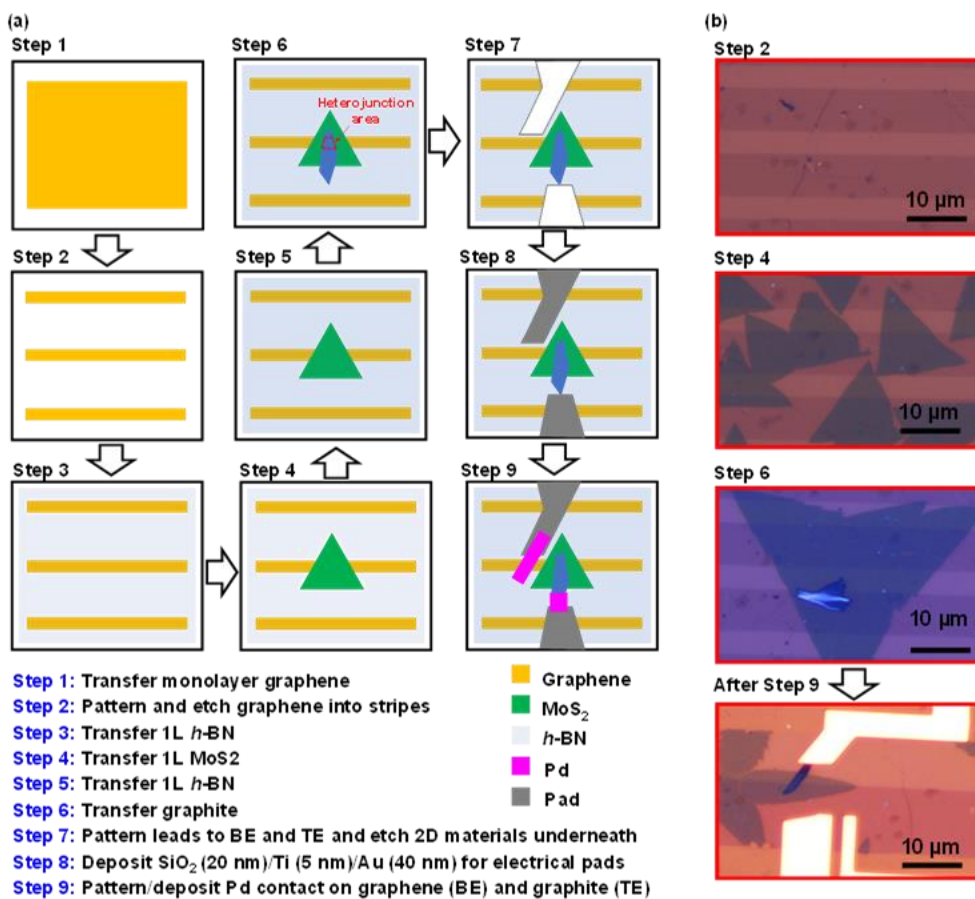
4.1 MoS$_2$ Transfer Process

Fig. S4. (a) Schematics of the fabrication steps for the H-shape heterojunction (b) The optical image of the device after Step 2, Step 4, Step 6 and Step 9.

The monolayer MoS_2 is grown directly on a SiO_2/Si substrate. We fabricate a transfer stamp by adhering a flat Polydimethylsiloxane (PDMS) layer to a glass slide (the size of the PDMS is around 2×2 cm) and then spin coat polypropylene carbonate (PPC) on top of the PDMS following by baking on a hot plate at 80 ºC for 5 minutes. Next, we gently adhere the stamp to the edge of the substrate where single-grain MoS_2 triangles are located (Step 1 of Fig. S4.1). Because SiO_2 is hydrophilic while MoS_2 is hydrophobic, after soaking the whole stack in water for an hour (Step 2 of Fig. S4.1), the MoS_2 layers will be released from the substrate while adhering to the stamp. After we remove the whole stack from the water and gently dry any remaining water droplets, we lift the stamp with MoS_2 from the substrate (Step 3 of Fig. S4.1). We bake the stamp at 80 ºC until the stamp is dry, typically 5 minutes (Step 4 of Fig. S4.1). Since multiple transfers are required for the final H-shape device, this baking (Step 4 of Fig. S4.1) is essential for reducing moisture contamination which can cause back-gate dielectric breakdown. Next, we adhere the stamp with isolated single-grained MoS_2 films onto the target chip and bake the sample on a hot plate for 5 minutes at 120 ºC to weaken the PPC adhesion to PDMS by reflowing the PPC. As a result, the MoS_2 layer and the PPC will stay on the target chip when we pull up the stamp (Step 5 of Fig. S4.1a). We note that the area with BE graphene stripes is around 2×2 mm, so an aligned transfer is not needed. Finally, we soak the target chip in acetone for a few hours to remove PPC and then rinse with isopropyl alcohol (IPA).
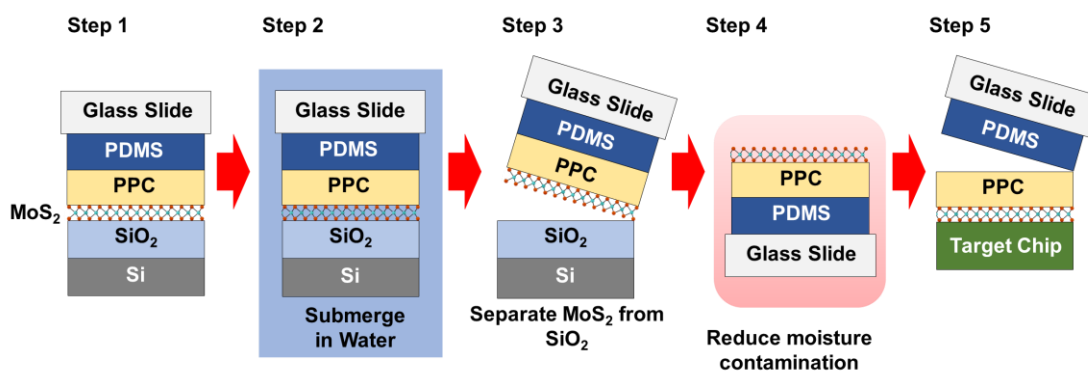

Fig. S4.1. Schematic of CVD MoS_2 transfer steps.

4.2 CVD Graphene Transfer Process

Continuous monolayer graphene is grown on copper foil. The stamp used for the graphene transfer process is very similar to the stamp used for the MoS_2 transfer, the only difference being that we spin coat a PMMA layer on top of the PDMS/PPC stamp, followed by baking at 80 ˚C for 5 minutes (Step 1 of Fig. S4.2a). We use this polymer bilayer as PMMA reflows at a higher temperature (~150 ˚C) than PPC (~120 ˚C), allowing us to release PPC while PMMA is still rigid. Keeping the polymer rigid is necessary for the graphene transfer as polymer reflow will tear monolayer graphene (0.3 nm), whereas thicker MoS_2 (0.615 nm) will

not be damaged. After adhering the stamp to the Cu foil and baking the whole stack on a hotplate at 80˚C for 5 minutes, we place the whole stack in a Cu etchant (ferric chloride solutions) for a few hours until the copper is etched completely (Step 2 of Fig. S4.2a) and then clean the stack by rinsing it in water multiple times (Step 3 of Fig. S4.2a). We then follow the similar process steps as in the MoS_2 transfer to release graphene onto the target chip (Step 4 of Fig. S4.2a). Figure S4.2c shows the optical image of intact graphene after transferred with double layer coating on the stamp.
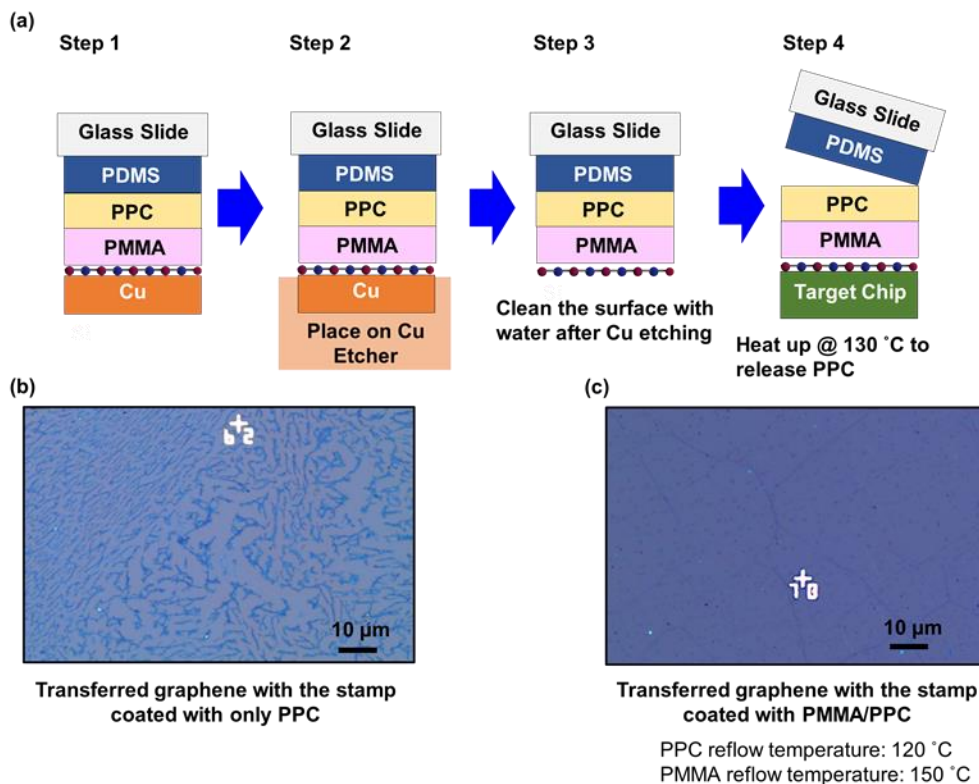

Fig. S4.2. (a) CVD monolayer graphene transfer steps. (b) Optical image of graphene transferred with only PPC layer on the stamp. (c) Optical image of intact graphene layer transferred with PPC/PMMA layer on the stamp.

4.3 *h*-BN Transfer Process

We grew continuous hexagonal boron nitride (*h*-BN) monolayers on reusable Pt foils at 1100 °C.[23] We then spin coat a PMMA layer onto the *h*-BN while it is still on the Pt foil. The entire structure (PMMA/*h*-BN/Pt) is attached to an electrode and submerged into a 1 M NaOH solution with a Pt mesh also submerged as the anode. Applying a voltage difference between the Pt foil substrate and Pt mesh induces H_2 bubbles, which delaminate the PMMA/*h*-BN from the Pt. Centimeter-scale *h*-BN films were transferred onto the target substrate, followed by baking on 80°C hot-plate for several minutes to remove the moisture and achieve *h*-

BN adhesion to the target substrate. After baking, we soak the target substrate in acetone for several hours to remove PMMA.

4.4 Graphite Transfer Process

In order to transfer exfoliated graphite onto the heterojunction, we prepare a bulb-like stamp so we can selectively transfer exfoliated flake with accurate alignment.[21] We cure a small PDMS droplet onto a flat PDMS/glass stack to create the bulb-like substrate and then spin coat this PDMS hemisphere with PPC. Next, we fix the stamp on a handle (glass slide) that is fixed to a micromanipulator. The handle is brought in contact with the substrate with exfoliated graphite flakes. After heating the stage up to 60˚C for 2 mins, the handle is detached to pick up exfoliated graphite on SiO_2 substrate. Next, the handle was brought in contact with the targeted heterojunction. We heat up the stage to 120˚C to release graphite and the PPC which can be easily removed by soaking in the acetone for 20 minutes.

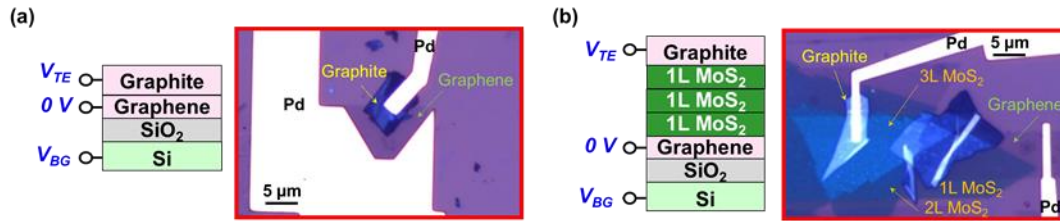## 5. Optical image of devices in Figure 2

Fig. S5. Optical images of devices in Fig. 2: (a) graphene-graphite, and (b) graphene-$3\times MoS_2$-graphite.

6. Asymmetric Heterojunction

For the symmetric H-shape, we clearly see a de-pinning effect with h-BN between MoS_2 and electrodes (graphene/graphite) as discussed in the main paper. To further study this de-pinning effect, we made additional devices with an asymmetric half H-shape structure (Fig. S6.1). This half H-shape device are stacks of h-BN (bottom)/MoS_2 (Top) (Fig. S6.1a,b) and MoS_2 (Bottom)/h-BN (Top) (Fig. S6.1c,d). Although one side of MoS_2 is pinned to graphene/graphite, the I-V_{TE} characteristics of both structures still exhibit bipolar diode behavior, indicating an existence of an energy barrier. Furthermore, the I-V_{BG} shows that MoS_2 energy barrier is also modulated by the V_{BG} as discussed in the H-shape device, suggesting that MoS_2 Fermi-level is de-pinned from its charge neutrality level (E_{CNL}), as illustrated in Fig. S6.2a. As the monolayer MoS_2

energy barrier is influenced by both interfaces, it appears that by de-pinning one side of the MoS_2 monolayer, we can still control part of its energy barrier.
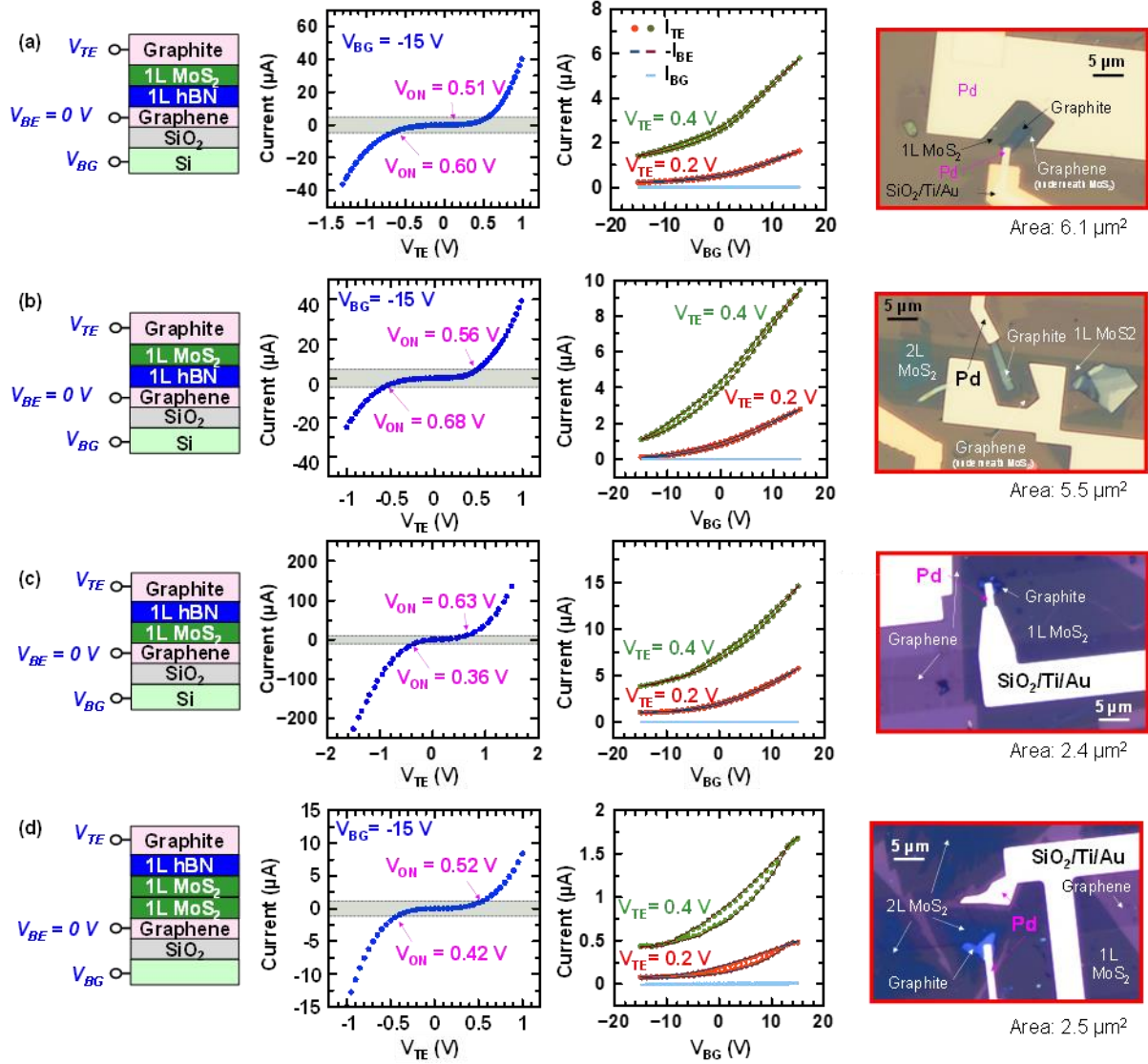

Fig. S6.1. Tunneling current measurement through the half H-shape (sample $1-4$), showing an intriguing phenomenon of the Fermi level de-pinning. (a) The measurement schematic of MoS_2 (Top)-h-BN (Bottom) heterojunction, I-V_{TE}, and I-V_{BG} of Sample 1. (b) The measurement schematic of MoS_2 (Top)-h-BN (Bottom) heterojunction, I-V_{TE}, and I-V_{BG} of Sample 2. (c) The measurement schematic of h-BN (Top)-MoS_2 (Bottom) heterojunction, I-V_{TE}, and I-V_{BG} of Sample 3. (d) The measurement schematic of h-BN (Top)-1L MoS_2-1L MoS_2 (Top) heterojunction, I-V_{TE}, and I-V_{BG} of Sample 4. The h-BN film has very low contrast under microscope thus is not visible in the optical image. All I-V_{BG} plots include currents from all three terminals, I_{TE}, I_{BE}, and I_{BG}, showing that the measured non-linearity is not due to gate leakage (*i.e.* I_{BG}). We examine every CVD film under microscope to confirm no visible tears/wrinkles near the heterojunction area.

Besides this interesting de-pinning effect, we observed a consistent asymmetric I-V_{TE} characteristic in the half H-shape device. As shown in Fig. S6.1, we defined the turn on voltage (V_{ON}) of the heterojunctions

as the V_{TE} at which the current reaches 10% of the maximum current (*i.e.* current at $V_{TE} = 1$ V). Comparing the V_{ON} of MoS$_2$ (bottom)-*h*-BN (top) (Fig. S6.1a,b) and MoS$_2$ (top)-*h*-BN (bottom) (Fig. S6.1c,d) shows that the V_{ON} is higher when electrons are injected through *h*-BN into MoS$_2$ barrier. For example, while applying positive V_{TE} on the asymmetric heterojunction *h*-BN (Bottom)-MoS$_2$ (Top), electrons flow from graphene into MoS$_2$ through *h*-BN, which acts as a series resistance and reduces the energy difference between the work function (WF) of graphene and conduction band (E_C) of MoS$_2$ (Fig. S6.2b), resulting in a smaller V$_{ON}$ than applying negative V_{TE}. Conversely, the heterojunction of MoS$_2$ (bottom)-*h*-BN (Top) has a higher V_{ON} when applying negative V_{TE} than positive V_{TE} with the same magnitude (Fig. S6.1c,d). To conclude, the V_{ON}'s in our heterojunctions are sensitive to the difference between the WF of graphene and E_C of MoS$_2$ at the same applied voltage.
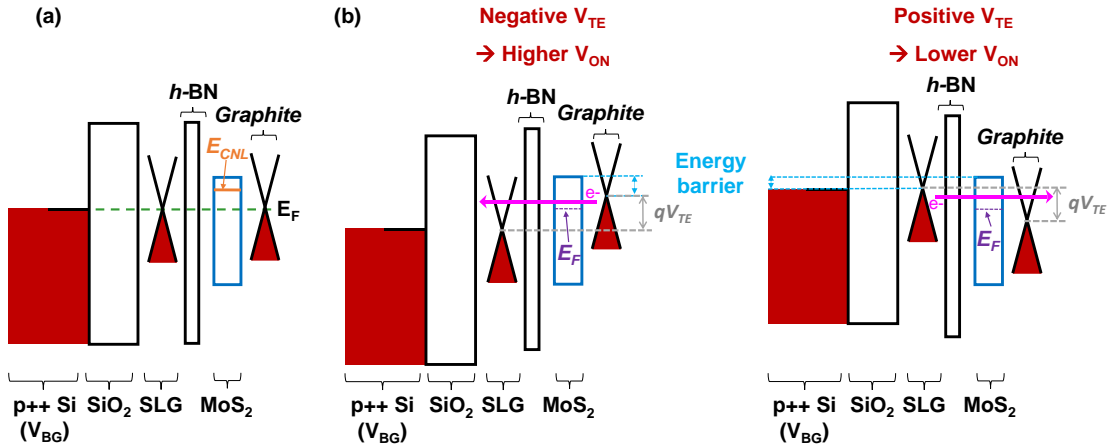

Fig. S6.2. (a) Energy band diagram of the *h*-BN (bottom)-MoS$_2$ (top), showing that E_F of MoS$_2$ is de-pinned from the E_{CNL}. (b) The energy barrier seen by electrons is the energy difference between graphene/graphite work function (WF) and MoS$_2$ E_C. The energy band diagrams at negative and positive V_{TE} with the same magnitude show the energy barrier seen by electrons is larger at negative V_{TE}, causing a higher V_{ON}.

7. Lateral Parasitic Resistances of the H-shape Device

Using graphene/graphite as electrodes allow us to fully characterize the tunneling current through vertical ultra-thin 2D material heterojunction, avoiding issues we discussed with MIM structures in Fig. S3. However, there are lateral parasitic resistances, such as graphene/graphite series resistance and Pd contact resistance. These lateral parasitic resistances can be estimated by the geometric shape of the device. In the optical image of our H-shape device (Fig. S7a), due to the irregular shape of the device, it is hard to estimate the equivalent contact width and graphene/graphite length. As such, by simplifying the geometric shape into Fig. S7b, we derived the upper bound of the lateral parasitic resistance (all colored resistances as shown in Fig. S7c). The value we use for the parasitic are summarized in Fig. S7c.[22,24 25] The total lateral resistance

therefore is 1000 $\Omega \cdot \mu m$ ($R_{Contact}$ of Pd) /1 μm (Pd contact width on graphene) + 1000 $\Omega \cdot \mu m$ ($R_{Contact}$ of Pd) / 2 μm (Pd contact width on graphite) + 1000 $\Omega/\square$ (R_{SH} of graphene) × 4 μm (Graphene length) / 1 μm (Graphene width) + 500 $\Omega/\square$ (R_{SH} of graphite) × 1 μm (Graphite length)/ 2 μm (Graphite width) = 5.75 kΩ.

With this value, we derive the I-V_{TE} data of the H-shape counting only black resistances as shown in Fig. S7c. As shown in Fig. S7d, the resistance of the whole H-shape is much larger than 6 kΩ, therefore the I-V_{TE} only changes slightly after subtracting 6 kΩ. If we assume an even higher parasitic resistance of 50 kΩ (the green line in Fig. S7d), the maximum current still only increases by 20% current. The conclusion here is that I-V_{TE} characteristics are dominated by vertical components (the black resistance as shown in Fig. S7c), not colored resistances. In order to increase selector current density in the future, the bottlenecks are 2D material quality and especially interfaces, and graphene/graphite vertical resistance.
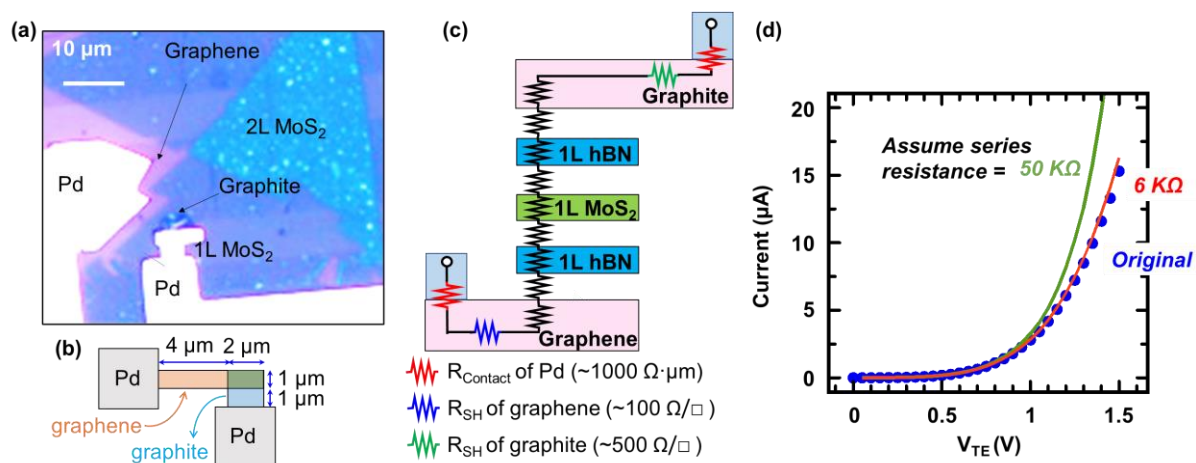

Fig. S7. (a) The optical image of the H-shape device. (b) The simplified geometric shape of the H-shape device for estimating the higher bound of the parasitic resistance. (c) The resistance components in the H-shape device. (c) The I-V_{TE} of the H-shape's experimental data, the extracted I-V_{TE} after subtracting 6 kΩ resistance, and the extracted I-V_{TE} after subtracting 50 kΩ resistance.

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