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Unipolar n-Type Black Phosphorus Transistors with Low Work Function Contacts

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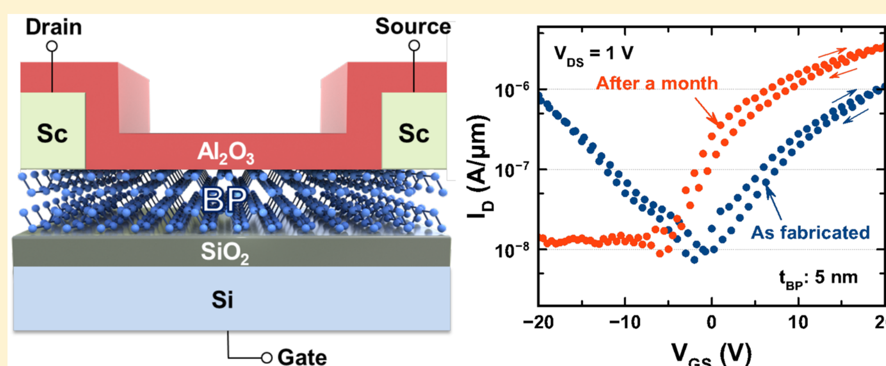
Supporting Information



ABSTRACT: Black phosphorus (BP) is a promising two-dimensional (2D) material for nanoscale transistors, due to its expected higher mobility than other 2D semiconductors. While most studies have reported ambipolar BP with a stronger p-type transport, it is important to fabricate both unipolar p- and n-type transistors for low-power digital circuits. Here, we report unipolar n-type BP transistors with low work function Sc and Er contacts, demonstrating a record high n-type current of 200 μA/μm in 6.5 nm thick BP. Intriguingly, the electrical transport of the as-fabricated, capped devices changes from ambipolar to n-type unipolar behavior after a month at room temperature. Transmission electron microscopy analysis of the contact cross-section reveals an intermixing layer consisting of partly oxidized metal at the interface. This intermixing layer results in a low n-type Schottky barrier between Sc and BP, leading to the unipolar behavior of the BP transistor. This unipolar transport with a suppressed p-type current is favorable for digital logic circuits to ensure a lower off-power consumption.

KEYWORDS: *Black phosphorus, scandium contact, erbium contact, low work function, transistors*

Since graphene was first isolated in 2004,[1] layered two-dimensional (2D) materials have attracted global attention due to their rich physics, including their mechanical, optical, electronic, and thermal properties. These properties are important for a variety of applications from computing to sensing and optoelectronics. For transistors that are suitable for mainstream digital logic circuits, it is essential for the material to have a band gap. The most studied 2D semiconductor, MoS_2, has been demonstrated to have an n-type current as high as 400 μA/μm (at V_{DS} = 2 V) for a monolayer and 830 μA/μm for 5−10 layer transistors (at V_{DS} = 1.5 V).[2,3] Black phosphorus (BP) is predicted to have a higher mobility than MoS_2 for both electrons and holes,[4] offering the possibility of a transistor technology with complementary n-type and p-type transistors with the same channel material. Several BP transistors have been reported,[5] with the highest on-current to date of ∼850 μA/μm (at V_{DS} = −1.8 V) for multilayer (8 nm thick) p-transistors.[6]

In addition to high mobility, BP is also expected to have a high saturation velocity (∼5.5 × 10^6 cm/s) compared to other 2D materials.[7] As 2D transistors continue to scale down in size, the output current will be increasingly limited by velocity saturation or ballistic effects, rather than pinch-off. These advantages make BP a promising candidate for future nanoelectronics.

Most BP transistors reported to date exhibit ambipolar electrical transport with positive threshold voltages due to its small band gap and Fermi level pinning at the contacts.[5,6,8] However, it is preferable to fabricate both n- and p-type devices using the same semiconductor material for a complementary transistor technology. The complementary transistors should also exhibit unipolar transport, a requirement for digital circuits to achieve a low off-power consumption.

Here, we demonstrate high-performance unipolar BP n-type transistors using low work function metal contacts (Sc and Er)

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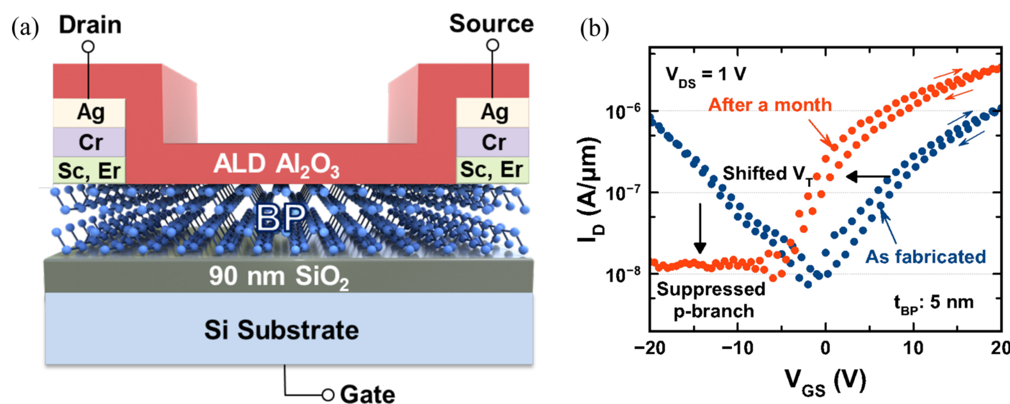

Figure 1. (a) A schematic illustration of Sc (or Er) contacts to the BP back-gate transistor on 30 or 90 nm SiO_2 with ALD Al_2O_3 capping. (b) A transfer curve of the Sc-BP device showing a transition after one month at room temperature with DC measurement. A suppressed p-branch and a threshold voltage shift were observed. The two measurements for each data set represent forward and backward sweeps (indicated by arrows), revealing a slight hysteretic behavior.

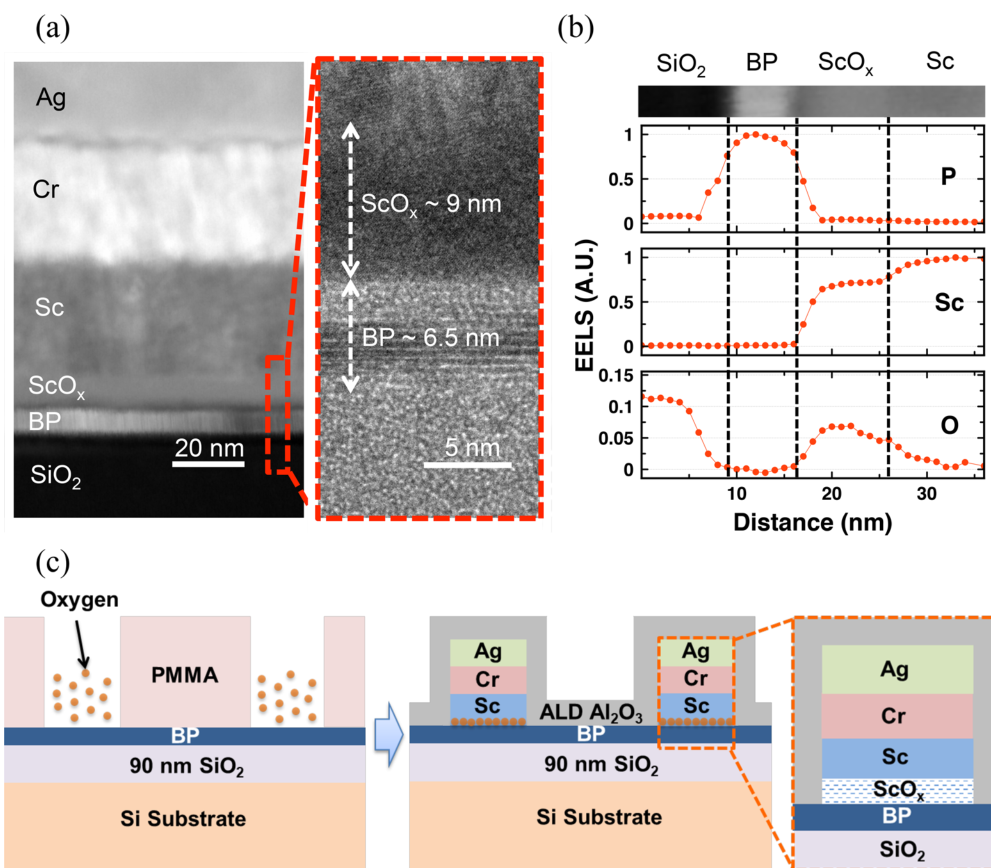

Figure 2. (a) TEM image of the contact cross-section with metal stacks Sc/Cr/Ag on BP, showing an intermixing layer (ScO_x). The inset is a zoomed-in TEM image of the dashed region. (b) Line scans across the contact layers using EELS element analysis (P, Sc, O), taken from the grayscale EELS data shown at top. The results were derived from two line scans due to EELS signal positions (1, P; 2, Sc and O). The units of the EELS signal were normalized, with the Sc and O signals taken together and normalized to the Sc maximum. (c) An illustration of intermixing layer formation during fabrication. First, oxygen remains in the contact regions after resist development in air. Second, the remaining oxygen was trapped at the contact interface after the metal deposition and ALD Al_2O_3 capping. Over time, the oxygen oxidized the Sc at the interface.

with Al_2O_3 encapsulation to prevent device oxidation. Over time, we observe a transition of the Sc-BP (and Er-BP) device electrical behavior from ambipolar to n-type unipolar transport. Transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) were employed to understand the cause of the transition. The observed effect is attributed to changes in the contact Schottky barrier height and contact doping. We compare these results with other n-type BP transistors to illustrate the progress that has been made toward a high-performance n-type BP transistor.

Figure 1a is a cross-sectional schematic of the back-gated BP device with Sc or Er (25 nm)/Cr (25 nm)/Ag (25 nm) metal stack contacts, capped with 20 nm atomic layer deposited (ALD) Al_2O_3. Due to the air sensitivity of BP[9,10] and Sc (or Er),[11] we

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fabricate the devices in an air-free environment,[12,13] apart from exposing the contact area to air for around 3 min before e-beam evaporation (Methods). The electrical stability due to ALD passivation for BP is well investigated.[9] Intriguingly, we observe that the device electrical transport has an ambipolar behavior immediately after fabrication, but changes to an n-type unipolar behavior after a month at room temperature in a nitrogen glovebox with ≤1 ppm of O_2 concentration. Figure 1b compares the transfer curves of the BP transistor with Sc contacts, measured right after fabrication and after a month, where I_D is the drain current, V_{GS} is the back-gate voltage (Si/SiO_2 substrate), and V_{DS} is the drain voltage (all referenced to the source voltage). The blue curve is measured immediately after fabrication, showing a clear ambipolar behavior, which suggests midgap Fermi level pinning. After a month stored at room temperature in the nitrogen glovebox, the device performance changed from ambipolar to n-type unipolar. We observed a suppressed p-branch current along with a negative threshold voltage shift. Since in this back-gated structure the global back-gate modulates contact resistance,[14] the low hole current and negative threshold voltage suggest a change of the Schottky barrier height (SBH) and contact doping. While this Letter mainly focuses on Sc-BP devices, the same electrical transition was observed in Er-BP devices as shown in the Supporting Information (Figure S4).

To investigate the cause of the change in behavior, we examine the cross-section of the contact region with TEM and EELS analysis. Figure 2a shows a cross-sectional TEM image of the Sc-BP contact, clearly showing an intermixing layer (∼9 nm) between BP and Sc, labeled as ScO_x. In the zoom-in image of the TEM, we observe 6.5 nm thick BP with the middle region showing crystalline layers, while the top and bottom regions were damaged from electron exposure during TEM imaging. To understand the composition of the intermixing layer, we use EELS to analyze the elements in each layer. Figure 2b shows an EELS line scan of the contact cross-section mapping to the TEM image. The EELS signal peaks of P, Sc, and O signals are at 450, 750, and 1450 eV, respectively. Due to the energy scan range limits, the P signal is from a separate scan than the Sc and O signals. This mapping reveals that the intermixing region contains mostly Sc and some O. As the O signal was much lower than the Sc signal, the layer is a substoichiometric ScO_x.

The EELS results give evidence that the composition of the intermixing layer is partly metal oxide, which is suspected to arise from brief air exposure (∼3 min) during the fabrication process. The capped Sc-BP (or Er-BP) devices are fabricated in an air-free environment, except for a brief period between resist development and contact metal deposition. Although the sample used for cross-sectional TEM analysis was exposed to air for a few minutes before loading into the TEM, we only detect the oxidized Sc at the contact interface. Figure 2c illustrates how this intermixing is formed during fabrication. After the contact regions are exposed to air between resist development and metal evaporation, oxygen remains in the contact regions. Subsequently, after metal deposition, this oxygen is trapped at the interface between Sc (or Er) and BP. During the ALD Al_2O_3 capping process after metal lift-off, the sample was heated at 150 °C for 2 h, assisting in oxygen diffusion into the Sc contacts, thus beginning the formation of a ∼9 nm metal oxide at the interface. As a result of the low oxygen content, this 9 nm thick ScO_x layer is likely to be electrically conductive. For our fabrication, oxygen remains at the Sc-BP interface, resulting in the Sc at this interface being the most oxidized. The change in electrical transport suggests that, for some devices, unreacted oxygen is still oxidizing Sc (or Er) over time at room temperature after fabrication. In addition, Sc and Er are both good oxygen getter metals.[15,16] Another good oxygen getter metal, Ti, has been used to reduce oxide layer thickness by extracting oxygen from oxide layers.[17] Similarly, the initial layers of Sc could extract oxygen from the BP oxide at the surface, which arises during the brief air exposure of BP contact areas as discussed earlier. This metal-oxide layer then depins the Schottky contact, providing a lower Schottky barrier for electrons (n-SBH) due to the low work functions of Sc and Er. In addition to the depinning effect, the substoichiometric metal-oxide dopes the contact,[18] thus shifting the threshold voltage for the back-gated transistor, where a back-gate voltage is required to turn on the Schottky contact.

Figure 3a shows the transfer curves of BP devices with V_{DS} ranging from 0.1 to 2 V for the BP transistor with a unipolar n-type behavior. Figure 3b shows the output current for BP thickness t_{BP} = 6.5 nm (L = 800 nm) and 4.5 nm (L = 580 nm), achieving 200 μA/μm and 125 μA/um, respectively. We did not observe current saturation from the pinch-off mechanism in these devices as $V_{DS} < (V_{GS} - V_T)$ for all measurements, primarily due to the thick gate oxide (90 and 30 nm for 6.5 and 4.5 nm BP, respectively) and negative V_T. However, pinch-off would be observed in these devices by using a thin gate dielectric to reduce $V_{GS} - V_T$. The 6.5 nm thick BP device is the sample we used for TEM and EELS analysis. Physical characterization and electrical analysis on the same device provides us with more reliable information about the intermixing layer.

In Figure 3c, we report the temperature dependence of the Sc-BP transfer curve. The schematic image of metal–insulator-semiconductor (MIS) contact band diagram in Figure 3c is based on the MIS study by Hu et al.[19] For the p-type current, there is a large temperature dependency, revealing a thermionic emission transport behavior and a larger Schottky barrier for holes. For the n-type current, we see a little temperature dependency, indicating a small Schottky barrier height for electrons and/or indicating a tunneling current through a smaller tunneling distance caused by oxygen contact doping. Both the p-type and n-type temperature behavior could be due to a combination of (1) Fermi level depinning and/or (2) contact doping.

To examine the Fermi level depinning effects individually, we use the analytical SBH extraction method reported by Penumatcha et al.[20] At a small V_{DS} value, this model assumes that the Schottky barriers limit the transmission through the device in the off-state and that carrier scattering inside the channel is negligible. To acquire a more comprehensive view of Fermi level pinning of different metals, we extract SBH for holes and electrons for several metals: Ti, Ni, Ag, Sc, and Er, as shown in Figure 4a. Figure 4b shows a schematic image of the work function of these metals compared to BP. The band gap of the multilayer BP is assumed to be ∼0.5 eV in the schematic image.[21,22] Due to midgap Fermi level pinning, Figure 4a,b shows that n-SBH and p-SBH are close in value for Ti, Ni, and Ag contacts, in contrast to Sc and Er. After the formation of the oxide layer, low work function metals (Sc and Er) could provide a much lower n-SBH, increasing the difference between n-SBH (∼0.1 eV) and p-SBH (∼0.4 eV) to provide a unipolar electrical transport.

Figure 4c shows two transfer curves of a Sc-BP device measured at V_{DS} = 0.1 V (blue, soon after fabrication; orange, after one month). The result shows no obvious SBH change in this device (blue p-SBH = 0.46 eV, n-SBH = 0.02 eV; orange p-SBH = 0.47 eV, n-SBH = 0.03 eV); however, the threshold voltage shifts by −8 V after one month. Thus, we can conclude

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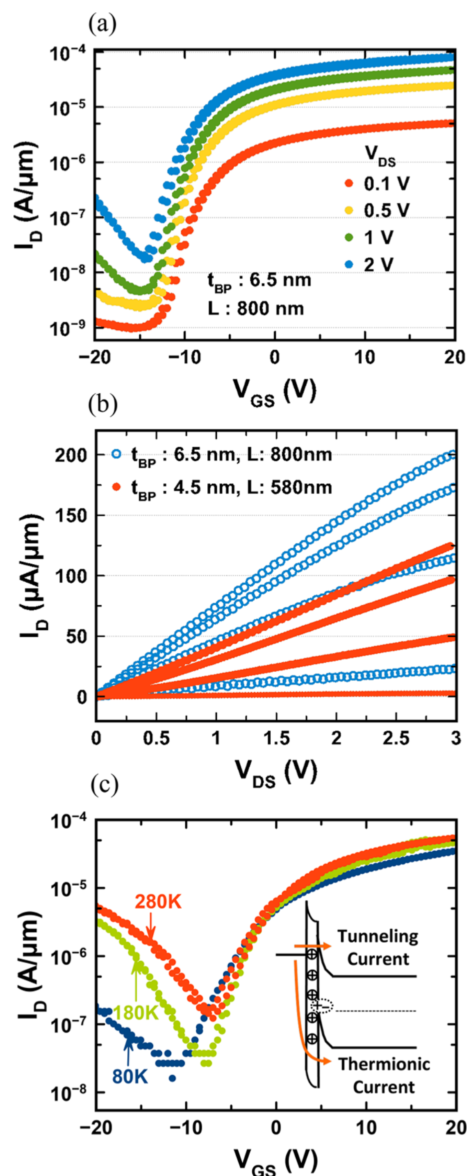

Figure 3. (a) Transfer curves of a Sc-BP device with 6.5 nm thick BP on 90 nm SiO_2 dielectric, at V_{DS} = 0.1, 0.5, 1, and 2 V. (b) The output current of 6.5 nm (V_{GS} = 5, 10, 15, 20 V) and 4.5 nm thick BP devices (V_{GS} = 0, 10, 20, 30 V) on 90 and 30 nm SiO_2 substrates, respectively. (c) The temperature dependence of the transfer curve of Sc-BP on 90 nm SiO_2. The stronger p-branch current dependence on temperature indicates thermionic current for holes from larger p-SBH, as depicted in the inset energy diagram. Data in this figure were taken by pulsed measurements with a forward−backward sweep.

that, for this particular device, the threshold voltage shift is due to contact doping, most likely from the oxidized metal (ScO_x), not Fermi level depinning.

There are two possible mechanisms for the observed n-doping of the contacts: (1) a fixed charge in the ScO_x layer can create remote charge doping,[23,24] and (2) when the phosphorus oxide loses oxygen to Sc, it leaves behind two electrons in the now ionic phosphorus. These extra electrons contribute to n-doping the contact.[25] Similar effects have been observed in Sc metal gates on HfO_2 gate dielectric, where a work function shift was also observed.[26]

Especially notable is the work by Li et al.,[8] which reported Sc contacts to BP with a high p-type on-current. The researchers exfoliated devices in air and measured their transport in a vacuum probe station, without capping. As we discuss in the Supporting Information (Figure S1), the air exposure time of BP is critical for the formation of the Sc-oxide layer for the n-type transistor behavior. The long air exposure during exfoliation in the work of Li et al.[8] could create BP oxide at the surface, inducing p-doping of the transistor channel and contact.[27,28] In contrast, in this work, only the contact area was exposed to air for ∼3 min, thus the channel of BP is primarily nonoxidized. Here we are able to measure a transition from ambipolar to n-type over time due to the ScO_x formation, while Li et al. only measured immediately after device fabrication. Finally, whereas Li et al. did not cap their BP devices, we capped ours with ALD Al_2O_3, and the capping is expected to enhance the n-type behavior in BP, as previously observed.[29] We also expect the ALD 150 °C deposition temperature to promote the ScO_x formation. In Figure S2, several more devices with the same transition are reported. Due to the in situ formation of ScO_x, our method results in varying ScO_x thickness. Future studies could focus on air-free evaporation processing with oxygen content control to improve the overall device and process variation.

Table 1 compares our results to literature, focusing on n-type BP devices with ambipolar or unipolar electrical transport.[30−34] All listed studies use ALD Al_2O_3 capping for air stability and n-channel doping. While our work has longer channel lengths, we demonstrate the highest n-type current drive while maintaining a max/min current ratio ≥ 10^4 for BP, also exhibiting a unipolar transport, which is needed (in addition to p-type) for complementary digital circuits with low-power operation.

Conclusions. In conclusion, we fabricated unipolar n-type BP transistors with low work function metals (Sc and Er), which demonstrate the highest unipolar n-type current drive (125 μA/μm and 200 μA/μm at V_{DS} = 3 V for 4.5 and 6.5 nm thick BP devices, respectively), while maintaining a 10^4 max/min current ratio. We uncover the role of ScO_x between the contacts and BP, which has two effects: (1) depinning of the low work function metal to BP and (2) n-doping the BP contacts. The n-type BP on-current reported here remains lower than the n-type current in MoS_2,[2,3] but significant progress has been made toward understanding and depinning n-type contacts in BP. This study provides a better understanding of 2D material doping and contacts and suggests pathways for the design of BP transistors for low-power logic circuits.

Materials and Methods. *BP Crystals.* Single crystal BP was purchased from Smart Elements.

Transistor Fabrication. The fabrication is completed in an air-free environment except exposing the contact area to air for ∼3 min between resist develop and metal evaporation. The process is as follows: (1) we mechanically exfoliate BP on SiO_2 dielectric (30 or 90 nm) on highly doped Si wafers (resistivity =1−5 mΩ·cm), in a nitrogen glovebox with ≤1 ppm of O_2 concentration and coat with poly(methyl methacrylate) resist (PMMA) to avoid oxidation. (2) We use electron-beam lithography to pattern the source and drain contacts, and (3) we deposit 25 nm Sc (or Er) and stable-metal capping layers in an ultrahigh vacuum electron-beam evaporator with a pressure of 5×10^{-11} Torr; (4) when returning to another glovebox connected to an ALD system, we perform metal lift-off and deposition of 20 nm Al_2O_3 at 150 °C by ALD.

Electrical Characterization. All electrical measurements were taken in a probe station, in a vacuum of $\sim 5 \times 10^{-5}$ Torr. For pulsed measurements, the pulse period was 10 ms and pulse width 5 ms to reduce hysteresis in electrical characterization.

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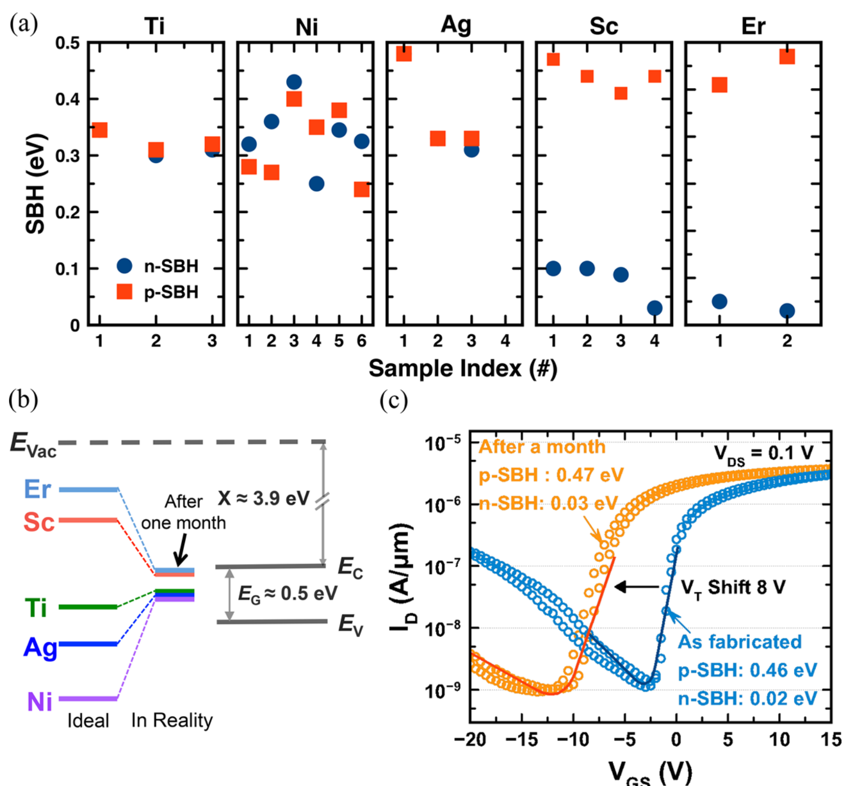

Figure 4. (a) A summary of the extracted Schottky barrier height (n-SBH, p-SBH) on Ni, Ag, Ti, Sc, and Er with ALD Al_2O_3 capping. The result shows midgap Fermi level pining for Ti, Ni, and Ag. On the other hand, for a low work function metal (Sc and Er), the intermixing layer with metal oxide might depin the Fermi level and separate the value of n-SBH and p-SBH. (b) Schematic view of metal work functions for Ni, Ag, Ti, and Sc, both for the ideal case and after a month. (c) Two transfer curves of the same device: after fabrication (p-SBH, 0.02 eV; n-SBH, 0.46 eV) and after a month (p-SBH, 0.03 eV; n-SBH, 0.47 eV). The SBH values are similar; however, the threshold voltage, V_T, shifts by −8 V. This significant threshold voltage shift indicates contact doping from ScO_x.

Table 1. Summary of n-Type BP Transistor Performance[a]

reference	transport	channel thickness (nm)	contact metal	channel treatment	channel length (nm)	V_{DS} (V)	max/min current ratio	current (μA/μm)
this work	unipolar	6.5	Sc/Cr/Ag	ALD Al_2O_3	800	3	10^4	200
						2	10^4	147
						1	10^4	75
		4.5	Sc/Cr/Au	ALD Al_2O_3	580	3	10^4	125
						2	10^4	85
						1	10^4	41
ref. 30	ambipolar	10 nm	Ti/Au	armchair and ALD Al_2O_3	300	2	10	200
					300	1	10	80
ref 31	unipolar	6	Al	ALD Al_2O_3	NA	1	10^4	12
ref 32	ambipolar	6.4	Ti/Au	ALD Al_2O_3	200	2	10	34
ref 33	ambipolar	8.6	Ni/Au	ALD Al_2O_3	200	2	10^3	86
ref 34	ambipolar	7	Ti/Au	Cu doping and ALD Al_2O_3	2 μm	2	10^3	0.7

[a]The present work achieves a record high output current (~200 μA/μm at V_{DS} = 3 V) with a 10^4 max/min current ratio and unipolar n-type transport for BP.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.7b05192

Electrical characterizations of different air-exposure times of BP contact area with Ni and Sc contacts, electrical characterizations of Er contact to BP, additional observed electrical transition on Sc-BP devices, and discussion of variation (PDF)

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Notes

The authors declare no competing financial interest.

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Supporting Information

Unipolar N-type Black Phosphorus Transistors with Low Work Function Contacts

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S1. Long air-exposure of contact area

The naturally formed ScO_x or ErO_x due to a brief air-exposure (~3 minutes) of contact area immediately before contact metal deposition is a primary contributor to the unipolar n-type transport. Thus, we extended the air exposure time of the contact area in order to ensure a uniform formation of the ScO_x or ErO_x layer. However, due to air sensitivity of BP, the longer air exposure time of the contact area can oxidize the BP surface and change the contact interface behavior.

To examine the influence of BP oxide on BP FETs, we first compared BP devices with Ni contacts with completely air free processing[1] and Ni-BP devices with the same processing, except the contact area was expose to air for around 10 minutes before Ni deposition. As shown in Fig. S1(a), the Ni-BP device with air-free evaporation demonstrates a more ambipolar electrical transport; in contrast, in Fig. S1(b) the device with ~10 minutes air exposure of contact area shows a more p-type unipolar electrical transport. This phenomenon can be explained by the BP oxide formed from longer air-exposure. This BP oxide can depin the BP Fermi-level and dope the contact p-type, since BP oxide exhibits a higher work function that results in charge transfer of holes from BP oxide to the BP channel.[2] Secondly, we fabricated Sc-BP devices with extended air-exposure of the contact area. Figure S1(c) is the result of a Sc-BP device shown in the main text, and Fig. S1(d) is a Sc-BP device with extending air-exposure time of the contact area to ~10 minutes instead of ~3 minutes. The Sc-BP device with longer air-exposure shows a more p-type transport behavior, similar to the Ni-BP device with extended air-exposure. Following the discussion for Ni-BP devices, the longer air exposure oxidizes the surface BP, therefore the naturally formed ScO_x and ErO_x is no longer contacting a pristine BP surface. The p-type transport indicates that the contact interface is influenced by BP oxide instead of ScO_x.

In addition to extending the air-exposure time of contacts, we also experimented with depositing an extra 0.5 nm ScO_x at the interface. We obtained ScO_x by first depositing 0.5 nm Sc at 10^{-7} Torr and then breaking vacuum. Due to the air sensitivity of Sc and high deposition pressure, the 0.5 nm of Sc will fully oxidize to form ScO_x. The electrical measurement results showed that all devices

suffered poor performance (I_D < 1 μA/μm with V_{DS} = 1 V). We believe this degradation is due to the large amount of oxygen from extended air exposure that then oxidizes both Sc and BP during the ALD process at the BP-Sc contact that creates a large electrical resistance. To conclude, the processing window is narrow for the formation of the ScO_x and ErO_x layer without also oxidizing the BP. Therefore, the environmental control and evaporation process used in this work is necessary to achieve unipolar n-type BP devices.

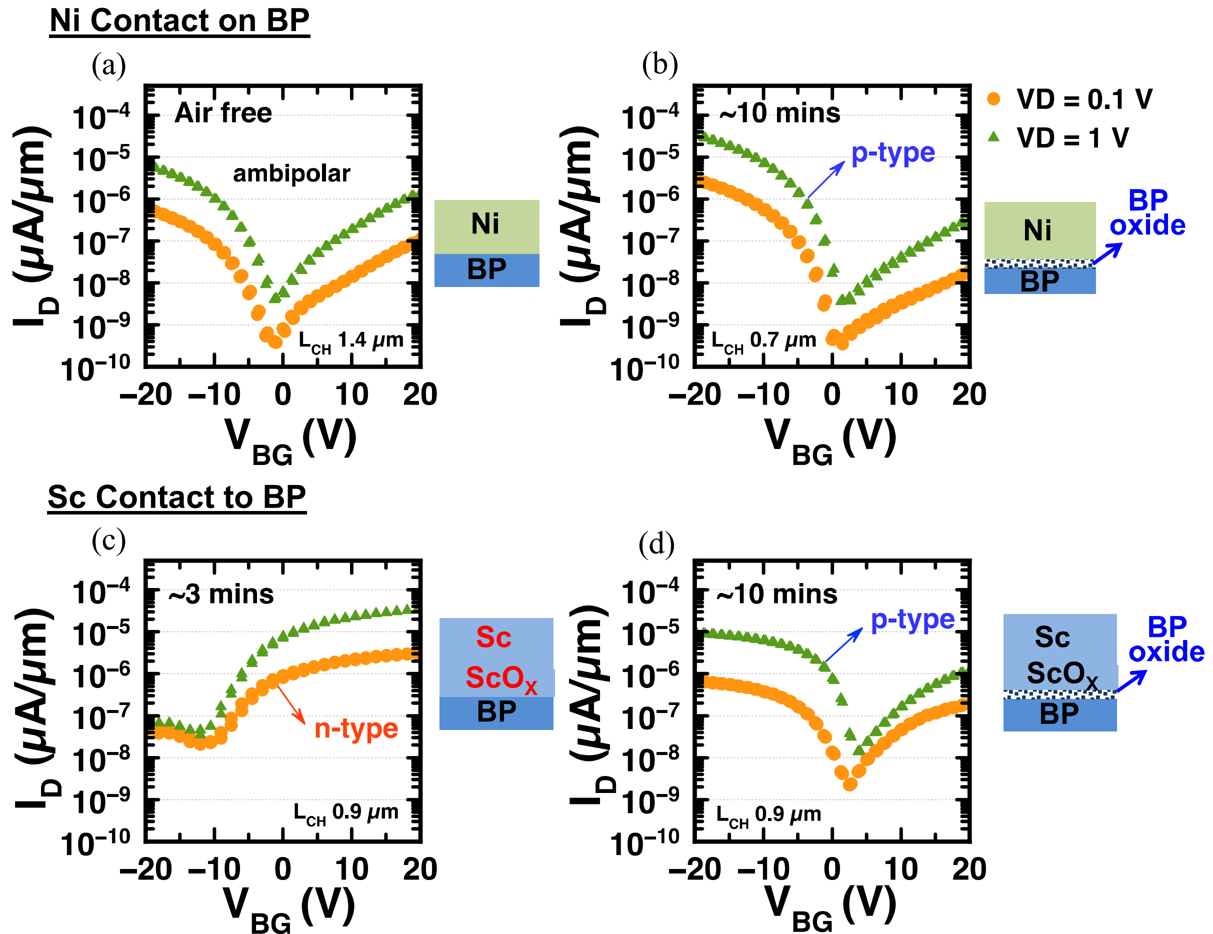


Fig. S1. Transfer curve comparison of BP devices with different air exposure amounts to the contact area before metal evaporation of Ni and Sc contacts. (a) Transfer curves of Ni contacts on BP with air-free evaporation. The air-free evaporation process ensures the contact area is never exposed to pressure below 1E-3 torr before metal evaporation. (b) Transfer curves of Ni contacts on BP with ~10 minutes air exposure of the contact area. (c, d) The transfer curve of Sc contacts on BP with only (c) ~3 minutes and (d) 10 minutes air exposure.

S2. Device variation

As discussed in S1, the air-exposure window for naturally forming ScO_x or ErO_x with pristine BP is narrow. Nevertheless, we observe an electrical transition of BP devices from ambipolar to n-type transistors. Figure S2 shows data from six additional devices to show that they all exhibit a similar electrical transition after one month. BP thickness of these samples ranges from 4.5 nm to 6.5 nm.

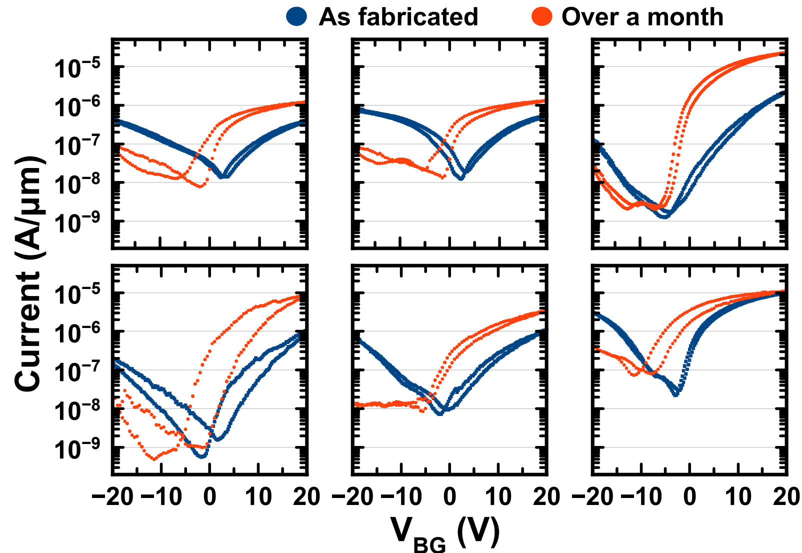


Fig. S2. Transfer curves of devices with clear electrical transitions. Channel length = 800 nm, V_{DS} = 1 V. Thickness of devices varies from 4.5 nm to 6.5 nm.

The naturally formed oxide in this work increases device-to-device fabrication variation, as the oxidation ratio and oxide thickness is not precisely controlled. In a back-gate transistor structure, Schottky contacts influence the threshold voltage of the devices. Therefore, with variation in the oxide thickness, the oxide depinning and doping effects varied for the different contacts, increasing the threshold voltage variation among devices. Also, it is likely that the oxidized layer is not completely uniform in oxygen concentration or thickness over the entire contact area in a single device, leading to variation within each contact. Figure S3(a) illustrates each contact as a set of several individual patches instead of a homogeneous contact area, with each patch having a different threshold voltage. Consequently, as these divided contact areas are electrically parallel with each other, the resultant subthreshold slope and on/off ratio for the device are degraded due to an averaging of transfer curves with different threshold voltages, as shown in Fig. S3(b).

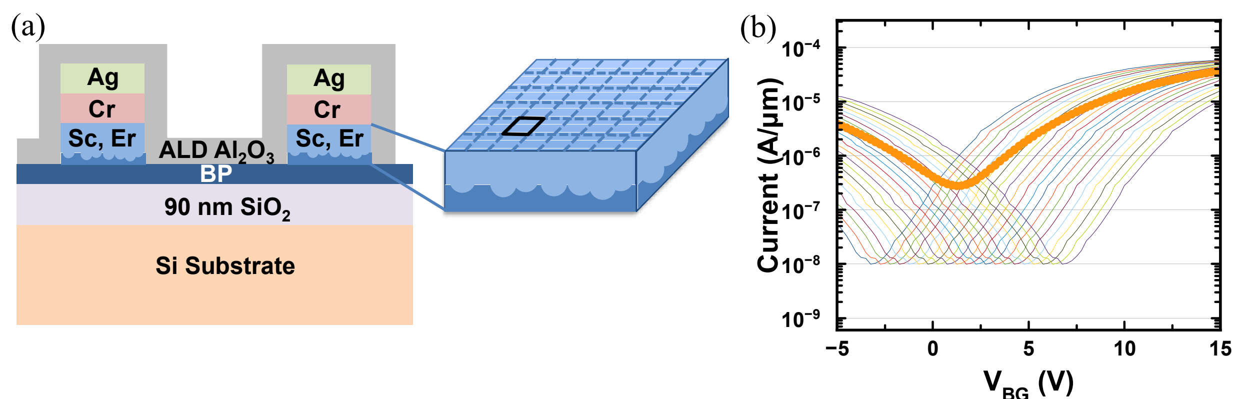


Fig. S3. (a) Illustration of uneven ScO_x or ErO_x, which can be treated as individual patches contributing different threshold voltages to a transfer curve. (b) Illustration of a transfer curve that adds up from the contribution of each individual patch. The transfer curves are for illustration only and are not individually measured. The device shows a lower on/off ratio and degraded subthreshold slope than the transfer curves contributed by the individual patches.

S3. Erbium Result

In addition to Sc-BP devices, we observed a similar electrical transition with another low work function metal, Er (work function: 3.16-3.2 eV). Figure S4(a) shows unipolar transport when the Er-contacted BP transistor was tested one month after device fabrication. The electrical transition over time is shown in Fig. S4(b). The transfer curve of Er devices shows a negative threshold voltage shift and a suppressed p-branch, similar to the Sc-contacted BP transistor.

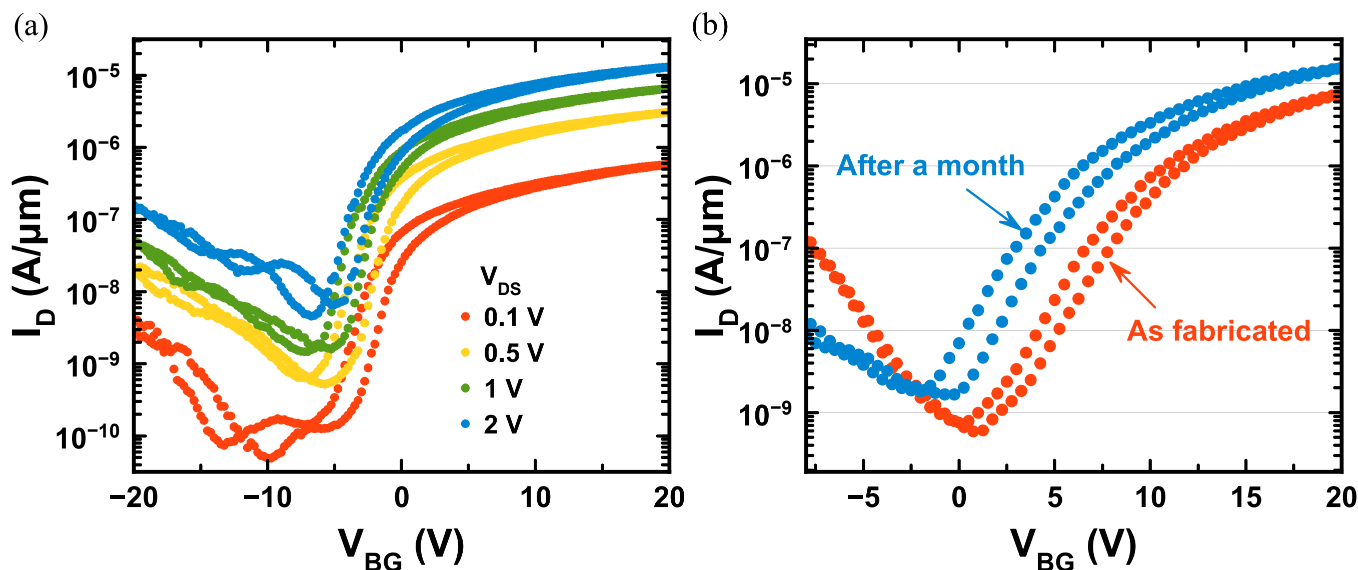
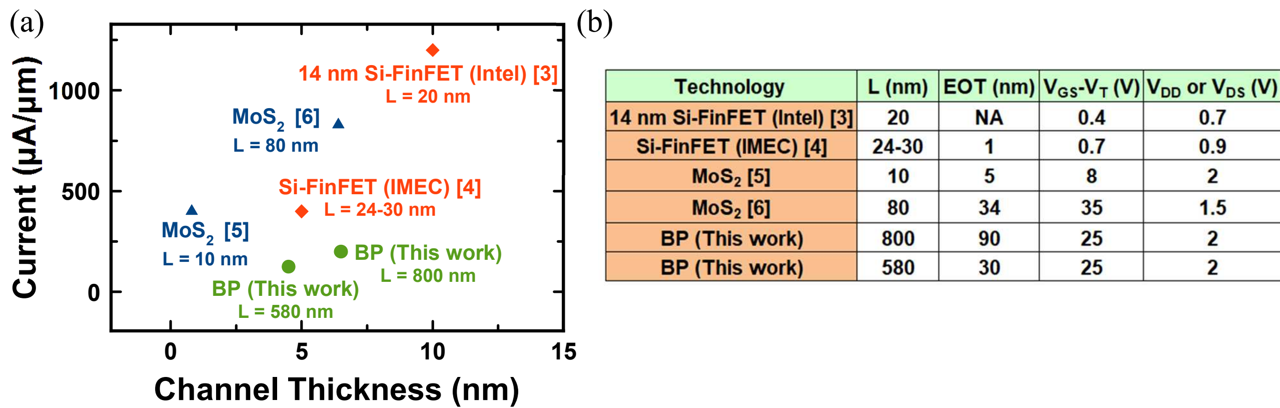


Fig. S4. (a) Transfer curves of a Er-BP device one month after fabrication, with unipolar n-type transport. (b) Transfer curves of a Er-BP device both as-fabricated and after a month, showing a clear electrical transition.

S4. NFET Comparison

While we have compared this work with other BP NFET in this paper, it is important to also benchmark this work with rival technologies. As one of the advantages of 2D material is its intrinsically thin channel thickness, which offers a better electrostatic control, Fig. 5 plots the drive current and thickness of Si-FinFET[3,4], MoS_2[5,6], and BP NFET. The n-type BP on-current reported here remains lower than n-type current in Si-FinFET and MoS_2. While part of the reasons why the current drive for BP in this work is lower is because of the longer gate lengths, we note that a low contact resistance is also needed for achieving higher drive current.



Technology	L (nm)	EOT (nm)	V_{GS}-V_T (V)	V_{DD} or V_{DS} (V)
14 nm Si-FinFET (Intel) [3]	20	NA	0.4	0.7
Si-FinFET (IMEC) [4]	24-30	1	0.7	0.9
MoS_2 [5]	10	5	8	2
MoS_2 [6]	80	34	35	1.5
BP (This work)	800	90	25	2
BP (This work)	580	30	25	2

Fig. S5. (a) NFET drive current comparison among a few different technologies as a function of channel thickness. (b) Channel length (L), equivalent oxide thickness (EOT), gate voltage overdrive (V_{GS}-V_T), and V_{DD} (or V_{DS}) for experimental data in (a).

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